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TITLE: CBP	ABBR: CBP
DRAWING: 411-001286-300A REV 0.0	ENGR: GOLENBIESKI
REVISED: Wed Jun 20 22:02:12 1990	PAGE: 1 OF 21

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 MB0 1P
 BOARD=NMB

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.
 SEC=1

GROUND ALL PINS ON THIS ROW!

101	1-101
102	1-102
103	1-103
104	1-104
105	1-105
106	1-106
107	1-107
108	1-108
109	1-109
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125	1-125
126	1-126
127	1-127
128	1-128
129	1-129
130	1-130
131	1-131
132	1-132
133	1-133
134	1-134
135	1-135
136	1-136P_MB0.PORTID<3>
137	1-137P_MB0.LED_INTL_OUT
138	1-138
139	1-139P_MB0.SLOTID<3>
140	1-140U_MB0.CLOCK_2X

201	1-201
202	1-202
203	1-203
204	1-204
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206	1-206
207	1-207
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229	1-229
230	1-230
231	1-231
232	1-232
233	1-233
234	1-234
235	1-235
236	1-236P_MB0.PORTID<2>
237	1-237P_MB0.LED_INTL_IN
238	1-238
239	1-239P_MB0.SLOTID<2>
240	1-240U_MB0.CLOCK_2X*

301	1-301
302	1-302
303	1-303
304	1-304
305	1-305
306	1-306
307	1-307
308	1-308
309	1-309
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330	1-330
331	1-331
332	1-332
333	1-333
334	1-334
335	1-335
336	1-336
337	1-337P_MB0.PORTID<1>
338	1-338
339	1-339P_MB0.SLOTID<1>
340	1-340

401	1-401
402	1-402
403	1-403
404	1-404
405	1-405
406	1-406
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424	1-424
425	1-425
426	1-426
427	1-427
428	1-428NMC_BYPASS
429	1-429
430	1-430
431	1-431
432	1-432
433	1-433
434	1-434
435	1-435
436	1-436
437	1-437P_MB0.PORTID<0>
438	1-438
439	1-439P_MB0.SLOTID<0>
440	1-440

501	1-501
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 DRAWING: 411-001286-300A Rev 0.0

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 ENGR: GOLENBIESKI

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AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 MB0 1P
 BOARD=NMB

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND
 TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.).
 THE GED 'SECTION' COMMAND WILL NOT WORK.
 SEC=2

GROUND ALL PINS
 ON THIS ROW!

101 2_101
 102 2_102
 103 2_103
 104 2_104
 105 2_105
 106 2_106
 107 2_107
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 109 2_109
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ABBR: CBP
 ENGR: GOLENBIESKI

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7

6

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1

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 MB0 1P
 BOARD=NMB

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE 'GED' SECTION COMMAND WILL NOT WORK.
 SEC=3

GROUND ALL PINS ON THIS ROW!

- 101 3_101
- 102 3_102
- 103 3_103
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8

7

6

3

2

1

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 MB0 154P
 BOARD=NMB

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.
 SEC=4

GROUND ALL PINS ON THIS ROW!

101	4_101	XSO_MB0.ADDR<10>	201	4_201	XSO_MB0.WR_DATA<8>	301	4_301	XSE_MB0.ADDR<10>	401	4_401	XSE_MB0.WR_DATA<8>	501	4_501	
102	4_102	XSO_MB0.ADDR<9>	202	4_202	XSO_MB0.WR_DATA<15>	302	4_302	XSE_MB0.ADDR<9>	402	4_402	XSE_MB0.WR_DATA<16>	502	4_502	
103	4_103		203	4_203	XSO_MB0.WR_DATA<24>	303	4_303		403	4_403	XSE_MB0.WR_DATA<24>	503	4_503	
104	4_104		204	4_204	XSO_MB0.WR_DATA<1>	304	4_304		404	4_404	XSE_MB0.WR_DATA<1>	504	4_504	
105	4_105	XSO_MB0.WR_DATA<9>	205	4_205	XSO_MB0.WR_DATA<17>	305	4_305	XSE_MB0.WR_DATA<9>	405	4_405	XSE_MB0.WR_DATA<17>	505	4_505	
106	4_106	XSO_MB0.WR_DATA<25>	206	4_206	XSO_MB0.WR_DATA<2>	306	4_306	XSE_MB0.WR_DATA<25>	406	4_406	XSE_MB0.WR_DATA<2>	506	4_506	
107	4_107	XSO_MB0.WR_DATA<10>	207	4_207	XSO_MB0.WR_DATA<18>	307	4_307	XSE_MB0.WR_DATA<10>	407	4_407	XSE_MB0.WR_DATA<18>	507	4_507	
108	4_108	XSO_MB0.WR_DATA<26>	208	4_208	XSO_MB0.WR_DATA<5>	308	4_308	XSE_MB0.WR_DATA<26>	408	4_408	XSE_MB0.WR_DATA<5>	508	4_508	
109	4_109	XSO_MB0.WR_DATA<13>	209	4_209	XSO_MB0.WR_DATA<21>	309	4_309	XSE_MB0.WR_DATA<13>	409	4_409	XSE_MB0.WR_DATA<21>	509	4_509	
110	4_110	XSO_MB0.WR_DATA<29>	210	4_210	XSO_MB0.WR_DATA<6>	310	4_310	XSE_MB0.WR_DATA<29>	410	4_410	XSE_MB0.WR_DATA<6>	510	4_510	
111	4_111	XSO_MB0.WR_DATA<14>	211	4_211	XSO_MB0.WR_DATA<22>	311	4_311	XSE_MB0.WR_DATA<14>	411	4_411	XSE_MB0.WR_DATA<22>	511	4_511	
112	4_112	XSO_MB0.WR_DATA<30>	212	4_212	XSO_MB0.WR_DATA<7>	312	4_312	XSE_MB0.WR_DATA<30>	412	4_412	XSE_MB0.WR_DATA<7>	512	4_512	
113	4_113	XSO_MB0.WR_DATA<15>	213	4_213	XSO_MB0.WR_DATA<23>	313	4_313	XSE_MB0.WR_DATA<15>	413	4_413	XSE_MB0.WR_DATA<23>	513	4_513	
114	4_114	XSO_MB0.WR_DATA<31>	214	4_214	XSO_MB0.WR_DATA<3>	314	4_314	XSE_MB0.WR_DATA<31>	414	4_414	XSE_MB0.WR_DATA<3>	514	4_514	
115	4_115	XSO_MB0.WR_DATA<11>	215	4_215	XSO_MB0.WR_DATA<19>	315	4_315	XSE_MB0.WR_DATA<11>	415	4_415	XSE_MB0.WR_DATA<19>	515	4_515	
116	4_116	XSO_MB0.WR_DATA<27>	216	4_216	XSO_MB0.WR_DATA<4>	316	4_316	XSE_MB0.WR_DATA<27>	416	4_416	XSE_MB0.WR_DATA<4>	516	4_516	
117	4_117	XSO_MB0.WR_DATA<12>	217	4_217	XSO_MB0.WR_DATA<20>	317	4_317	XSE_MB0.WR_DATA<12>	417	4_417	XSE_MB0.WR_DATA<20>	517	4_517	
118	4_118	XSO_MB0.WR_DATA<28>	218	4_218	XSO_MB0.WR_PAR<0>	318	4_318	XSE_MB0.WR_DATA<28>	418	4_418	XSE_MB0.WR_PAR<0>	518	4_518	
119	4_119	XSO_MB0.WR_PAR<1>	219	4_219	XSO_MB0.WR_PAR<2>	319	4_319	XSE_MB0.WR_PAR<1>	419	4_419	XSE_MB0.WR_PAR<2>	519	4_519	
120	4_120	XSO_MB0.WR_PAR<3>	220	4_220		320	4_320	XSE_MB0.WR_PAR<3>	420	4_420		520	4_520	
121	4_121	96P	221	4_221	145P	321	4_321	129P	421	4_421	129P	521	4_521	
122	4_122		222	4_222		322	4_322		422	4_422		522	4_522	
123	4_123		223	4_223		323	4_323		423	4_423		523	4_523	
124	4_124		224	4_224		324	4_324		424	4_424		524	4_524	
125	4_125		225	4_225	MB0_XSO.BANK_DONE<7..0>	325	4_325	MB0_XSE.BANK_DONE<15..0>	425	4_425	MB0_XSE.BANK_DONE<7..0>	525	4_525	
126	4_126	MB0_XSO.BANK_DONE<15..0>	226	4_226		326	4_326		426	4_426		526	4_526	
127	4_127		227	4_227		327	4_327		427	4_427		527	4_527	
128	4_128		228	4_228		328	4_328		428	4_428		528	4_528	
129	4_129		229	4_229		329	4_329		429	4_429		529	4_529	
130	4_130		230	4_230		330	4_330		430	4_430		530	4_530	
131	4_131		231	4_231		331	4_331	XC_MB0.RAM_RFSH	431	4_431		531	4_531	
132	4_132		232	4_232		332	4_332		432	4_432		532	4_532	
133	4_133	XSOE_MB0.SPARE1	233	4_233		333	4_333	XSE_MB0.REF_REQ	433	4_433		533	4_533	
134	4_134	XSOE_MB0.SPARE0	234	4_234		334	4_334	XSO_MB0.REF_REQ	434	4_434	XSO0_MB0.SPARE1	534	4_534	
135	4_135	XSIE_MB0.SPARE1	235	4_235		335	4_335		435	4_435	XSO0_MB0.SPARE0	535	4_535	
136	4_136	XSIE_MB0.SPARE0	236	4_236		336	4_336		436	4_436	XSIO_MB0.SPARE1	536	4_536	
137	4_137	MB0_XSIE.SEND_PAR_ERR	237	4_237		337	4_337	MB0_XC.SOFT_ERROR	437	4_437	XSIO_MB0.SPARE0	537	4_537	
138	4_138	MB0_XSIO.SEND_PAR_ERR	238	4_238		338	4_338		438	4_438	XC_MB0.SYS_RUN*	538	4_538	
139	4_139	MB0_XSOE.SEND_PAR_ERR	239	4_239	M_CST.CERR_E	339	4_339		439	4_439	XC_MB0.LOG_RUN*	539	4_539	
140	4_140	MB0_XSO0.SEND_PAR_ERR	240	4_240	M_CST.CERR_O	340	4_340		440	4_440		540	4_540	

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 ENGR: GOLENBIESKI
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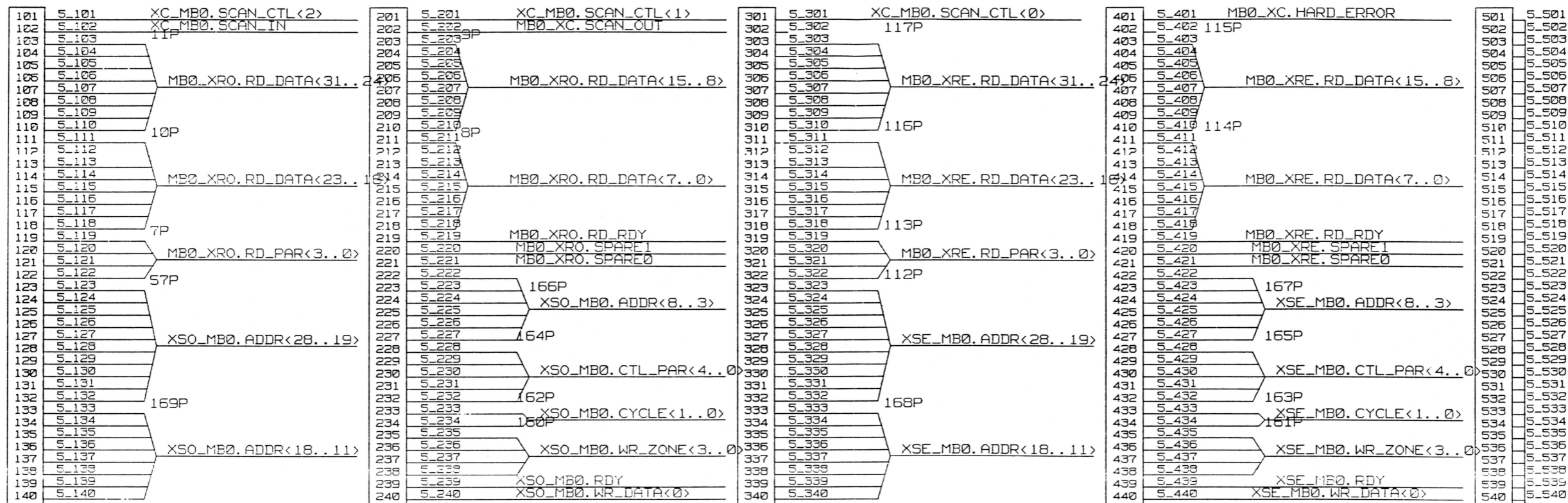
AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 MB0 174P
 BOARD=NMB

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.

SEC=5

GROUND ALL PINS ON THIS ROW!



GND\G

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TITLE: CBP
 DRAWING: 411-001286-300A Rev 0.0

ABBR: CBP
 ENGR: GOLENBIESKI

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1

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 SP0 82P
 BOARD=NSP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.

SEC=1

GROUND ALL PINS ON THIS ROW!

101	1.101
102	1.102
103	1.103
104	1.104
105	1.105
106	1.106
107	1.107
108	1.108
109	1.109
110	1.110
111	1.111
112	1.112
113	1.113
114	1.114
115	1.115
116	1.116
117	1.117
118	1.118
119	1.119
120	1.120
121	1.121
122	1.122
123	1.123
124	1.124
125	1.125
126	1.126
127	1.127
128	1.128
129	1.129
130	1.130
131	1.131
132	1.132
133	1.133
134	1.134
135	1.135
136	1.136 BP_SP0.PORTID<3>
137	1.137 SP0_BP.LBD_INTL_OUT
138	1.138
139	1.139 BP_SP0.SLOTID<3>
140	1.140 CU_SP0.CLOCK_2X

201	1.201
202	1.202
203	1.203
204	1.204
205	1.205
206	1.206
207	1.207
208	1.208
209	1.209
210	1.210
211	1.211
212	1.212
213	1.213
214	1.214
215	1.215
216	1.216
217	1.217
218	1.218
219	1.219
220	1.220
221	1.221
222	1.222
223	1.223
224	1.224
225	1.225
226	1.226
227	1.227
228	1.228
229	1.229
230	1.230
231	1.231
232	1.232
233	1.233
234	1.234
235	1.235
236	1.236 BP_SP0.PORTID<2>
237	1.237 BP_SP0.LBD_INTL_IN
238	1.238
239	1.239 BP_SP0.SLOTID<2>
240	1.240 CU_SP0.CLOCK_2X*

301	1.301 UP0_SP0.IDLE
302	1.302
303	1.303
304	1.304
305	1.305
306	1.306
307	1.307
308	1.308
309	1.309
310	1.310
311	1.311
312	1.312
313	1.313
314	1.314
315	1.315
316	1.316
317	1.317
318	1.318
319	1.319
320	1.320
321	1.321
322	1.322
323	1.323
324	1.324
325	1.325
326	1.326
327	1.327
328	1.328
329	1.329
330	1.330
331	1.331
332	1.332
333	1.333
334	1.334
335	1.335
336	1.336
337	1.337 BP_SP0.PORTID<1>
338	1.338
339	1.339 BP_SP0.SLOTID<1>
340	1.340

401	1.401 SP0_UP0.DISP_EP<10>
402	1.402 SP0_UP0.DISP_EP<9>
403	1.403 SP0_UP0.DISP_EP<8>
404	1.404 SP0_UP0.DISP_EP<7>
405	1.405 SP0_UP0.DISP_EP<6>
406	1.406 SP0_UP0.DISP_EP<5>
407	1.407 SP0_UP0.DISP_EP<4>
408	1.408 SP0_UP0.DISP_EP<3>
409	1.409 SP0_UP0.DISP_EP<2>
410	1.410 SP0_UP0.DISP_EP<1>
411	1.411 SP0_UP0.DISP_EP<0>
412	1.412 SP0_UP0.DISP_IREG<2>
413	1.413 SP0_UP0.DISP_IREG<1>
414	1.414 SP0_UP0.DISP_IREG<0>
415	1.415 SP0_UP0.DISP_JREG<2>
416	1.416 SP0_UP0.DISP_JREG<1>
417	1.417 SP0_UP0.DISP_JREG<0>
418	1.418 SP0_UP0.DISP_KREG<2>
419	1.419 SP0_UP0.DISP_KREG<1>
420	1.420 SP0_UP0.DISP_KREG<0>
421	1.421
422	1.422 SP0_UP0.IEEE
423	1.423
424	1.424
425	1.425
426	1.426
427	1.427
428	1.428
429	1.429
430	1.430
431	1.431
432	1.432
433	1.433
434	1.434
435	1.435
436	1.436
437	1.437 BP_SP0.PORTID<0>
438	1.438
439	1.439 BP_SP0.SLOTID<0>
440	1.440

501	1.501
502	1.502
503	1.503
504	1.504
505	1.505
506	1.506
507	1.507
508	1.508
509	1.509
510	1.510
511	1.511
512	1.512
513	1.513
514	1.514
515	1.515
516	1.516
517	1.517
518	1.518
519	1.519
520	1.520
521	1.521
522	1.522
523	1.523
524	1.524
525	1.525
526	1.526
527	1.527
528	1.528
529	1.529
530	1.530
531	1.531
532	1.532
533	1.533
534	1.534
535	1.535
536	1.536
537	1.537
538	1.538
539	1.539
540	1.540 GND\G

SECTION 1 (BOTTOM)

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TITLE: CBP
 DRAWING: 411-001286-300A Rev 0.0

ABBR: CBP
 ENGR: GOLENBIESKI

REVISED: Thu Jun 21 09:33:20 1990

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2

1

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 SP0 90P
 BOARD=NSP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE 'GED' SECTION COMMAND WILL NOT WORK.

SEC=2

GROUND ALL PINS ON THIS ROW!

101	2_101	XRO_SP0_RD_DATA<5>
102	2_102	XRO_SP0_RD_DATA<6>
103	2_103	XRO_SP0_RD_DATA<7>
104	2_104	XRO_SP0_RD_DATA<13>
105	2_105	XRO_SP0_RD_DATA<14>
106	2_106	XRO_SP0_RD_DATA<15>
107	2_107	XRO_SP0_RD_DATA<21>
108	2_108	XRO_SP0_RD_DATA<22>
109	2_109	XRO_SP0_RD_DATA<23>
110	2_110	XRO_SP0_RD_DATA<29>
111	2_111	XRO_SP0_RD_DATA<30>
112	2_112	XRO_SP0_RD_DATA<31>
113	2_113	XRE_SP0_RD_DATA<5>
114	2_114	XRE_SP0_RD_DATA<6>
115	2_115	XRE_SP0_RD_DATA<7>
116	2_116	XRE_SP0_RD_DATA<13>
117	2_117	XRE_SP0_RD_DATA<14>
118	2_118	XRE_SP0_RD_DATA<15>
119	2_119	XRE_SP0_RD_DATA<21>
120	2_120	XRE_SP0_RD_DATA<22>
121	2_121	XRE_SP0_RD_DATA<23>
122	2_122	XRE_SP0_RD_DATA<29>
123	2_123	XRE_SP0_RD_DATA<30>
124	2_124	XRE_SP0_RD_DATA<31>
125	2_125	
126	2_126	
127	2_127	
128	2_128	
129	2_129	
130	2_130	
131	2_131	
132	2_132	
133	2_133	
134	2_134	
135	2_135	
136	2_136	
137	2_137	VP0_SP0_SPARE3
138	2_138	VP0_SP0_SPARE2
139	2_139	VP0_SP0_SPARE1
140	2_140	VP0_SP0_SPARE0

201	2_201	SP0_XSO_WR_DATA<5>
202	2_202	SP0_XSO_WR_DATA<6>
203	2_203	SP0_XSO_WR_DATA<7>
204	2_204	SP0_XSO_WR_DATA<13>
205	2_205	SP0_XSO_WR_DATA<14>
206	2_206	SP0_XSO_WR_DATA<15>
207	2_207	SP0_XSO_WR_DATA<21>
208	2_208	SP0_XSO_WR_DATA<22>
209	2_209	SP0_XSO_WR_DATA<23>
210	2_210	SP0_XSO_WR_DATA<29>
211	2_211	SP0_XSO_WR_DATA<30>
212	2_212	SP0_XSO_WR_DATA<31>
213	2_213	SP0_XSE_WR_DATA<5>
214	2_214	SP0_XSE_WR_DATA<6>
215	2_215	SP0_XSE_WR_DATA<7>
216	2_216	SP0_XSE_WR_DATA<13>
217	2_217	SP0_XSE_WR_DATA<14>
218	2_218	SP0_XSE_WR_DATA<15>
219	2_219	SP0_XSE_WR_DATA<21>
220	2_220	SP0_XSE_WR_DATA<22>
221	2_221	SP0_XSE_WR_DATA<23>
222	2_222	SP0_XSE_WR_DATA<29>
223	2_223	SP0_XSE_WR_DATA<30>
224	2_224	SP0_XSE_WR_DATA<31>
225	2_225	
226	2_226	
227	2_227	
228	2_228	
229	2_229	
230	2_230	
231	2_231	
232	2_232	
233	2_233	
234	2_234	
235	2_235	
236	2_236	
237	2_237	
238	2_238	
239	2_239	
240	2_240	

301	2_301	VP0_SP0_DATA<5>
302	2_302	VP0_SP0_DATA<6>
303	2_303	VP0_SP0_DATA<7>
304	2_304	VP0_SP0_DATA<13>
305	2_305	VP0_SP0_DATA<14>
306	2_306	VP0_SP0_DATA<15>
307	2_307	VP0_SP0_DATA<21>
308	2_308	VP0_SP0_DATA<22>
309	2_309	VP0_SP0_DATA<23>
310	2_310	VP0_SP0_DATA<29>
311	2_311	VP0_SP0_DATA<30>
312	2_312	VP0_SP0_DATA<31>
313	2_313	VP0_SP0_DATA<37>
314	2_314	VP0_SP0_DATA<38>
315	2_315	VP0_SP0_DATA<39>
316	2_316	VP0_SP0_DATA<45>
317	2_317	VP0_SP0_DATA<46>
318	2_318	VP0_SP0_DATA<47>
319	2_319	VP0_SP0_DATA<53>
320	2_320	VP0_SP0_DATA<54>
321	2_321	VP0_SP0_DATA<55>
322	2_322	VP0_SP0_DATA<61>
323	2_323	VP0_SP0_DATA<62>
324	2_324	VP0_SP0_DATA<63>
325	2_325	
326	2_326	
327	2_327	
328	2_328	
329	2_329	
330	2_330	VP0_SP0_MXV_REQ_NEXT
331	2_331	VP0_SP0_SXV_REQ_NEXT
332	2_332	
333	2_333	VP0_SP0_PSW_HAZ
334	2_334	VP0_SP0_SET_FDZ
335	2_335	VP0_SP0_SET_FSN
336	2_336	VP0_SP0_SET_OV
337	2_337	VP0_SP0_SET_RO
338	2_338	VP0_SP0_SET_SDZ
339	2_339	VP0_SP0_SET_SIV
340	2_340	VP0_SP0_SET_UN

401	2_401	SP0_VP0_DATA<5>
402	2_402	SP0_VP0_DATA<6>
403	2_403	SP0_VP0_DATA<7>
404	2_404	SP0_VP0_DATA<13>
405	2_405	SP0_VP0_DATA<14>
406	2_406	SP0_VP0_DATA<15>
407	2_407	SP0_VP0_DATA<21>
408	2_408	SP0_VP0_DATA<22>
409	2_409	SP0_VP0_DATA<23>
410	2_410	SP0_VP0_DATA<29>
411	2_411	SP0_VP0_DATA<30>
412	2_412	SP0_VP0_DATA<31>
413	2_413	SP0_VP0_DATA<37>
414	2_414	SP0_VP0_DATA<38>
415	2_415	SP0_VP0_DATA<39>
416	2_416	SP0_VP0_DATA<45>
417	2_417	SP0_VP0_DATA<46>
418	2_418	SP0_VP0_DATA<47>
419	2_419	SP0_VP0_DATA<53>
420	2_420	SP0_VP0_DATA<54>
421	2_421	SP0_VP0_DATA<55>
422	2_422	SP0_VP0_DATA<61>
423	2_423	SP0_VP0_DATA<62>
424	2_424	SP0_VP0_DATA<63>
425	2_425	
426	2_426	
427	2_427	
428	2_428	
429	2_429	
430	2_430	
431	2_431	
432	2_432	SP0_VP0_DISP_RDY
433	2_433	SP0_VP0_DISP_PSW_HAZ
434	2_434	
435	2_435	
436	2_436	
437	2_437	
438	2_438	
439	2_439	
440	2_440	

501	2_501	
502	2_502	
503	2_503	
504	2_504	
505	2_505	
506	2_506	
507	2_507	
508	2_508	
509	2_509	
510	2_510	
511	2_511	
512	2_512	
513	2_513	
514	2_514	
515	2_515	
516	2_516	
517	2_517	
518	2_518	
519	2_519	
520	2_520	
521	2_521	
522	2_522	
523	2_523	
524	2_524	
525	2_525	
526	2_526	
527	2_527	
528	2_528	
529	2_529	
530	2_530	
531	2_531	
532	2_532	
533	2_533	
534	2_534	
535	2_535	
536	2_536	
537	2_537	
538	2_538	
539	2_539	
540	2_540	GND\G

SECTION 2

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TITLE: CBP
 DRAWING: 411-001286-300A Rev 0.0

ABBR: CBP
 ENGR: GOLENBIESKI

REVISED: Thu Jun 21 09:33:42 1990

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2

1

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 SP0 77P

BOARD=NSP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND
 TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.).
 THE GED 'SECTION' COMMAND WILL NOT WORK.

SEC=3

GROUND ALL PINS
ON THIS ROW!

101	3_101	XRO_SP0_RD_DATA<2>
102	3_102	XRO_SP0_RD_DATA<3>
103	3_103	XRO_SP0_RD_DATA<4>
104	3_104	XRO_SP0_RD_DATA<10>
105	3_105	XRO_SP0_RD_DATA<11>
106	3_106	XRO_SP0_RD_DATA<12>
107	3_107	XRO_SP0_RD_DATA<18>
108	3_108	XRO_SP0_RD_DATA<19>
109	3_109	XRO_SP0_RD_DATA<20>
110	3_110	XRO_SP0_RD_DATA<26>
111	3_111	XRO_SP0_RD_DATA<27>
112	3_112	XRO_SP0_RD_DATA<28>
113	3_113	XRE_SP0_RD_DATA<2>
114	3_114	XRE_SP0_RD_DATA<3>
115	3_115	XRE_SP0_RD_DATA<4>
116	3_116	XRE_SP0_RD_DATA<10>
117	3_117	XRE_SP0_RD_DATA<11>
118	3_118	XRE_SP0_RD_DATA<12>
119	3_119	XRE_SP0_RD_DATA<18>
120	3_120	XRE_SP0_RD_DATA<19>
121	3_121	XRE_SP0_RD_DATA<20>
122	3_122	XRE_SP0_RD_DATA<26>
123	3_123	XRE_SP0_RD_DATA<27>
124	3_124	XRE_SP0_RD_DATA<28>
125	3_125	
126	3_126	
127	3_127	
128	3_128	
129	3_129	
130	3_130	
131	3_131	
132	3_132	VP0_SP0_UXA_ADDR<PAR<0>
133	3_133	VP0_SP0_UXA_ADDR<24>
134	3_134	VP0_SP0_UXA_ADDR<25>
135	3_135	VP0_SP0_UXA_ADDR<26>
136	3_136	VP0_SP0_UXA_ADDR<27>
137	3_137	VP0_SP0_UXA_ADDR<28>
138	3_138	VP0_SP0_UXA_ADDR<29>
139	3_139	VP0_SP0_UXA_ADDR<30>
140	3_140	VP0_SP0_UXA_ADDR<31>

201	3_201	SP0_XSO_WR_DATA<2>
202	3_202	SP0_XSO_WR_DATA<3>
203	3_203	SP0_XSO_WR_DATA<4>
204	3_204	SP0_XSO_WR_DATA<10>
205	3_205	SP0_XSO_WR_DATA<11>
206	3_206	SP0_XSO_WR_DATA<12>
207	3_207	SP0_XSO_WR_DATA<18>
208	3_208	SP0_XSO_WR_DATA<19>
209	3_209	SP0_XSO_WR_DATA<20>
210	3_210	SP0_XSO_WR_DATA<26>
211	3_211	SP0_XSO_WR_DATA<27>
212	3_212	SP0_XSO_WR_DATA<28>
213	3_213	SP0_XSE_WR_DATA<2>
214	3_214	SP0_XSE_WR_DATA<3>
215	3_215	SP0_XSE_WR_DATA<4>
216	3_216	SP0_XSE_WR_DATA<10>
217	3_217	SP0_XSE_WR_DATA<11>
218	3_218	SP0_XSE_WR_DATA<12>
219	3_219	SP0_XSE_WR_DATA<18>
220	3_220	SP0_XSE_WR_DATA<19>
221	3_221	SP0_XSE_WR_DATA<20>
222	3_222	SP0_XSE_WR_DATA<26>
223	3_223	SP0_XSE_WR_DATA<27>
224	3_224	SP0_XSE_WR_DATA<28>
225	3_225	
226	3_226	
227	3_227	
228	3_228	
229	3_229	
230	3_230	
231	3_231	
232	3_232	VP0_SP0_UXA_ADDR<PAR<1>
233	3_233	VP0_SP0_UXA_ADDR<16>
234	3_234	VP0_SP0_UXA_ADDR<17>
235	3_235	VP0_SP0_UXA_ADDR<18>
236	3_236	VP0_SP0_UXA_ADDR<19>
237	3_237	VP0_SP0_UXA_ADDR<20>
238	3_238	VP0_SP0_UXA_ADDR<21>
239	3_239	VP0_SP0_UXA_ADDR<22>
240	3_240	VP0_SP0_UXA_ADDR<23>

301	3_301	VP0_SP0_DATA<2>
302	3_302	VP0_SP0_DATA<3>
303	3_303	VP0_SP0_DATA<4>
304	3_304	VP0_SP0_DATA<10>
305	3_305	VP0_SP0_DATA<11>
306	3_306	VP0_SP0_DATA<12>
307	3_307	VP0_SP0_DATA<18>
308	3_308	VP0_SP0_DATA<19>
309	3_309	VP0_SP0_DATA<20>
310	3_310	VP0_SP0_DATA<26>
311	3_311	VP0_SP0_DATA<27>
312	3_312	VP0_SP0_DATA<28>
313	3_313	VP0_SP0_DATA<34>
314	3_314	VP0_SP0_DATA<35>
315	3_315	VP0_SP0_DATA<36>
316	3_316	VP0_SP0_DATA<42>
317	3_317	VP0_SP0_DATA<43>
318	3_318	VP0_SP0_DATA<44>
319	3_319	VP0_SP0_DATA<50>
320	3_320	VP0_SP0_DATA<51>
321	3_321	VP0_SP0_DATA<52>
322	3_322	VP0_SP0_DATA<58>
323	3_323	VP0_SP0_DATA<59>
324	3_324	VP0_SP0_DATA<60>
325	3_325	
326	3_326	
327	3_327	
328	3_328	
329	3_329	
330	3_330	
331	3_331	
332	3_332	
333	3_333	
334	3_334	
335	3_335	
336	3_336	
337	3_337	
338	3_338	
339	3_339	
340	3_340	

401	3_401	SP0_VP0_DATA<2>
402	3_402	SP0_VP0_DATA<3>
403	3_403	SP0_VP0_DATA<4>
404	3_404	SP0_VP0_DATA<10>
405	3_405	SP0_VP0_DATA<11>
406	3_406	SP0_VP0_DATA<12>
407	3_407	SP0_VP0_DATA<18>
408	3_408	SP0_VP0_DATA<19>
409	3_409	SP0_VP0_DATA<20>
410	3_410	SP0_VP0_DATA<26>
411	3_411	SP0_VP0_DATA<27>
412	3_412	SP0_VP0_DATA<28>
413	3_413	SP0_VP0_DATA<34>
414	3_414	SP0_VP0_DATA<35>
415	3_415	SP0_VP0_DATA<36>
416	3_416	SP0_VP0_DATA<42>
417	3_417	SP0_VP0_DATA<43>
418	3_418	SP0_VP0_DATA<44>
419	3_419	SP0_VP0_DATA<50>
420	3_420	SP0_VP0_DATA<51>
421	3_421	SP0_VP0_DATA<52>
422	3_422	SP0_VP0_DATA<58>
423	3_423	SP0_VP0_DATA<59>
424	3_424	SP0_VP0_DATA<60>
425	3_425	
426	3_426	
427	3_427	
428	3_428	
429	3_429	
430	3_430	
431	3_431	
432	3_432	
433	3_433	
434	3_434	
435	3_435	
436	3_436	
437	3_437	
438	3_438	
439	3_439	SP0_VP0_CNTL<1>
440	3_440	SP0_VP0_CNTL<0>

501	3_501	
502	3_502	
503	3_503	
504	3_504	
505	3_505	
506	3_506	
507	3_507	
508	3_508	
509	3_509	
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526	3_526	
527	3_527	
528	3_528	
529	3_529	
530	3_530	
531	3_531	
532	3_532	
533	3_533	
534	3_534	
535	3_535	
536	3_536	
537	3_537	
538	3_538	
539	3_539	
540	3_540	GNDNG

SECTION 3

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CONVEX

TITLE: CBP
 DRAWING: 411-001286-300A Rev 0.0
 REVISED: Thu Jun 21 09:34:06 1990

ABBR: CBP
 ENGR: GOLENBIESKI

PAGE: 9 of 21

8

7

6

3

2

1

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 SP0 36P
 BOARD=NSP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.

SEC=4

GROUND ALL PINS ON THIS ROW!

101	4_101 SP0_XSE, CTL_PAR<4>
102	4_102 SP0_XSE, CTL_PAR<3>
103	4_103 SP0_XSE, CTL_PAR<2>
104	4_104 SP0_XSE, CTL_PAR<1>
105	4_105 SP0_XSE, CTL_PAR<0>
106	4_106 SP0_XSE, WR_ZONE<3>
107	4_107 SP0_XSE, WR_ZONE<2>
108	4_108 SP0_XSE, WR_ZONE<1>
109	4_109 SP0_XSE, WR_ZONE<0>
110	4_110
111	4_111
112	4_112
113	4_113
114	4_114
115	4_115
116	4_116
117	4_117 SP0_UP0, SPARE3
118	4_118 SP0_UP0, SPARE2
119	4_119 SP0_UP0, SPARE1
120	4_120 SP0_UP0, SPARE0
121	4_121
122	4_122
123	4_123 UP0_SP0, UXA_ADDR<3>
124	4_124 UP0_SP0, UXA_ADDR<0>
125	4_125 UP0_SP0, UXA_ADDR<1>
126	4_126 UP0_SP0, UXA_ADDR<2>
127	4_127 UP0_SP0, UXA_ADDR<3>
128	4_128 UP0_SP0, UXA_ADDR<4>
129	4_129 UP0_SP0, UXA_ADDR<5>
130	4_130 UP0_SP0, UXA_ADDR<6>
131	4_131 UP0_SP0, UXA_ADDR<7>
132	4_132 UP0_SP0, UXA_ADDR<2>
133	4_133 UP0_SP0, UXA_ADDR<8>
134	4_134 UP0_SP0, UXA_ADDR<9>
135	4_135 UP0_SP0, UXA_ADDR<10>
136	4_136 UP0_SP0, UXA_ADDR<11>
137	4_137 UP0_SP0, UXA_ADDR<12>
138	4_138 UP0_SP0, UXA_ADDR<13>
139	4_139 UP0_SP0, UXA_ADDR<14>
140	4_140 UP0_SP0, UXA_ADDR<15>

201	4_201 SP0_XSE, CYCLE<0>
202	4_202 SP0_XSE, CYCLE<1>
203	4_203 SP0_XSE, BD_SEL<0>
204	4_204 SP0_XSE, BD_SEL<1>
205	4_205 SP0_XSE, BD_SEL<2>
206	4_206 SP0_XSE, BD_SEL<3>
207	4_207 SP0_XSE, ADDR<3>
208	4_208 SP0_XSE, ADDR<4>
209	4_209 SP0_XSE, ADDR<5>
210	4_210 SP0_XSE, ADDR<6>
211	4_211 SP0_XSE, ADDR<7>
212	4_212 SP0_XSE, ADDR<8>
213	4_213 SP0_XSE, ADDR<9>
214	4_214 SP0_XSE, ADDR<10>
215	4_215 SP0_XSE, ADDR<11>
216	4_216 SP0_XSE, ADDR<12>
217	4_217 SP0_XSE, ADDR<13>
218	4_218 SP0_XSE, ADDR<14>
219	4_219 SP0_XSE, ADDR<15>
220	4_220 SP0_XSE, ADDR<16>
221	4_221 SP0_XSE, ADDR<17>
222	4_222 SP0_XSE, ADDR<18>
223	4_223 SP0_XSE, ADDR<19>
224	4_224 SP0_XSE, ADDR<20>
225	4_225 SP0_XSE, ADDR<21>
226	4_226 SP0_XSE, ADDR<22>
227	4_227 SP0_XSE, ADDR<23>
228	4_228 SP0_XSE, ADDR<24>
229	4_229 SP0_XSE, ADDR<25>
230	4_230 SP0_XSE, ADDR<26>
231	4_231 SP0_XSE, ADDR<27>
232	4_232 SP0_XSE, ADDR<28>
233	4_233
234	4_234
235	4_235
236	4_236
237	4_237
238	4_238
239	4_239
240	4_240

301	4_301 SP0_XSO, CTL_PAR<4>
302	4_302 SP0_XSO, CTL_PAR<3>
303	4_303 SP0_XSO, CTL_PAR<2>
304	4_304 SP0_XSO, CTL_PAR<1>
305	4_305 SP0_XSO, CTL_PAR<0>
306	4_306 SP0_XSO, WR_ZONE<3>
307	4_307 SP0_XSO, WR_ZONE<2>
308	4_308 SP0_XSO, WR_ZONE<1>
309	4_309 SP0_XSO, WR_ZONE<0>
310	4_310
311	4_311
312	4_312
313	4_313
314	4_314
315	4_315
316	4_316
317	4_317
318	4_318
319	4_319
320	4_320
321	4_321
322	4_322
323	4_323
324	4_324
325	4_325 XC_SP0, TRAP_VECT<0>
326	4_326 XC_SP0, TRAP_VECT<1>
327	4_327 XC_SP0, TRAP_VECT<2>
328	4_328 XC_SP0, TRAP_VECT<3>
329	4_329 XC_SP0, TRAP_TYPE<0>
330	4_330 XC_SP0, TRAP_TYPE<1>
331	4_331 XC_SP0, TRAP_TYPE<2>
332	4_332 XC_SP0, TRAP_TYPE<3>
333	4_333 XC_SP0, TRAP_VECT<4>
334	4_334 XC_SP0, TRAP_VECT<5>
335	4_335 XC_SP0, TRAP_VECT<6>
336	4_336 XC_SP0, TRAP_VECT<7>
337	4_337 XC_SP0, TRAP_VECT<8>
338	4_338 XC_SP0, TRAP_VECT<9>
339	4_339 XC_SP0, TRAP_VECT<10>
340	4_340 XC_SP0, TRAP_VECT<11>

401	4_401 SP0_XSO, CYCLE<0>
402	4_402 SP0_XSO, CYCLE<1>
403	4_403 SP0_XSO, BD_SEL<0>
404	4_404 SP0_XSO, BD_SEL<1>
405	4_405 SP0_XSO, BD_SEL<2>
406	4_406 SP0_XSO, BD_SEL<3>
407	4_407 SP0_XSO, ADDR<3>
408	4_408 SP0_XSO, ADDR<4>
409	4_409 SP0_XSO, ADDR<5>
410	4_410 SP0_XSO, ADDR<6>
411	4_411 SP0_XSO, ADDR<7>
412	4_412 SP0_XSO, ADDR<8>
413	4_413 SP0_XSO, ADDR<9>
414	4_414 SP0_XSO, ADDR<10>
415	4_415 SP0_XSO, ADDR<11>
416	4_416 SP0_XSO, ADDR<12>
417	4_417 SP0_XSO, ADDR<13>
418	4_418 SP0_XSO, ADDR<14>
419	4_419 SP0_XSO, ADDR<15>
420	4_420 SP0_XSO, ADDR<16>
421	4_421 SP0_XSO, ADDR<17>
422	4_422 SP0_XSO, ADDR<18>
423	4_423 SP0_XSO, ADDR<19>
424	4_424 SP0_XSO, ADDR<20>
425	4_425 SP0_XSO, ADDR<21>
426	4_426 SP0_XSO, ADDR<22>
427	4_427 SP0_XSO, ADDR<23>
428	4_428 SP0_XSO, ADDR<24>
429	4_429 SP0_XSO, ADDR<25>
430	4_430 SP0_XSO, ADDR<26>
431	4_431 SP0_XSO, ADDR<27>
432	4_432 SP0_XSO, ADDR<28>
433	4_433
434	4_434
435	4_435
436	4_436
437	4_437
438	4_438
439	4_439
440	4_440

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538	4_538
539	4_539
540	4_540 GND\G

SECTION 4

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TITLE: CBP
 DRAWING: 411-001285-300A Rev 0.0

ABBR: CBP
 ENGR: GOLENBIESKI

REVISED: Thu Jun 21 09:34:29 1990

PAGE: 10 of 21

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 SP0 109P

BOARD=NSP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.

SEC=5

GROUND ALL PINS ON THIS ROW!

101	5_101	XC_SP0_SCAN_CTL<2>
102	5_102	XC_SP0_SCAN_IN
103	5_103	XRE_SP0_RD_RDY
104	5_104	XRO_SP0_RD_RDY
105	5_105	XSO_SP0_A_REQ_NEXT
106	5_106	XSO_SP0_A_REQ_PEND
107	5_107	XSO_SP0_A_ST_PEND
108	5_108	XSO_SP0_B_REQ_NEXT
109	5_109	XSO_SP0_B_REQ_PEND
110	5_110	XSO_SP0_B_ST_PEND
111	5_111	XSE_SP0_A_REQ_NEXT
112	5_112	XSE_SP0_A_REQ_PEND
113	5_113	XSE_SP0_A_ST_PEND
114	5_114	XSE_SP0_B_REQ_NEXT
115	5_115	XSE_SP0_B_REQ_PEND
116	5_116	XSE_SP0_B_ST_PEND
117	5_117	XRO_SP0_RD_PAR<3>
118	5_118	XRO_SP0_RD_DATA<0>
119	5_119	XRO_SP0_RD_DATA<1>
120	5_120	XRO_SP0_RD_PAR<2>
121	5_121	XRO_SP0_RD_DATA<8>
122	5_122	XRO_SP0_RD_DATA<9>
123	5_123	XRO_SP0_RD_PAR<1>
124	5_124	XRO_SP0_RD_DATA<16>
125	5_125	XRO_SP0_RD_DATA<17>
126	5_126	XRO_SP0_RD_PAR<0>
127	5_127	XRO_SP0_RD_DATA<24>
128	5_128	XRO_SP0_RD_DATA<25>
129	5_129	XRE_SP0_RD_PAR<3>
130	5_130	XRE_SP0_RD_DATA<0>
131	5_131	XRE_SP0_RD_DATA<1>
132	5_132	XRE_SP0_RD_PAR<2>
133	5_133	XRE_SP0_RD_DATA<8>
134	5_134	XRE_SP0_RD_DATA<9>
135	5_135	XRE_SP0_RD_PAR<1>
136	5_136	XRE_SP0_RD_DATA<16>
137	5_137	XRE_SP0_RD_DATA<17>
138	5_138	XRE_SP0_RD_PAR<0>
139	5_139	XRE_SP0_RD_DATA<24>
140	5_140	XRE_SP0_RD_DATA<25>

201	5_201	XC_SP0_SCAN_CTL<1>
202	5_202	SP0_XC_SCAN_OUT
203	5_203	SP0_XSE_RDY
204	5_204	SP0_XSO_RDY
205	5_205	SP0_XRE_RTN_PAR_ERR
206	5_206	SP0_XRO_RTN_PAR_ERR
207	5_207	
208	5_208	SP0_XC_DEADLOCK
209	5_209	SP0_XC_TRAP_COMP
210	5_210	SP0_XC_HW_HUNG
211	5_211	XC_SP0_TRAP_RDY
212	5_212	XC_SP0_MT_COMP
213	5_213	XC_SP0_CU_STATUS_EN
214	5_214	XC_SP0_CU_STATUS
215	5_215	XC_SP0_USEC_EN
216	5_216	
217	5_217	SP0_XSO_WR_PAR<3>
218	5_218	SP0_XSO_WR_DATA<0>
219	5_219	SP0_XSO_WR_DATA<1>
220	5_220	SP0_XSO_WR_PAR<2>
221	5_221	SP0_XSO_WR_DATA<8>
222	5_222	SP0_XSO_WR_DATA<9>
223	5_223	SP0_XSO_WR_PAR<1>
224	5_224	SP0_XSO_WR_DATA<16>
225	5_225	SP0_XSO_WR_DATA<17>
226	5_226	SP0_XSO_WR_PAR<0>
227	5_227	SP0_XSO_WR_DATA<24>
228	5_228	SP0_XSO_WR_DATA<25>
229	5_229	SP0_XSE_WR_PAR<3>
230	5_230	SP0_XSE_WR_DATA<0>
231	5_231	SP0_XSE_WR_DATA<1>
232	5_232	SP0_XSE_WR_PAR<2>
233	5_233	SP0_XSE_WR_DATA<8>
234	5_234	SP0_XSE_WR_DATA<9>
235	5_235	SP0_XSE_WR_PAR<1>
236	5_236	SP0_XSE_WR_DATA<16>
237	5_237	SP0_XSE_WR_DATA<17>
238	5_238	SP0_XSE_WR_PAR<0>
239	5_239	SP0_XSE_WR_DATA<24>
240	5_240	SP0_XSE_WR_DATA<25>

301	5_301	XC_SP0_SCAN_CTL<0>
302	5_302	VP0_SP0_DISP_REQ_NEXT
303	5_303	
304	5_304	VP0_SP0_UXM_RDY
305	5_305	VP0_SP0_UXS_RDY
306	5_306	VP0_SP0_UXA_VM<0>
307	5_307	VP0_SP0_UXA_VM<1>
308	5_308	VP0_SP0_UXA_LAST
309	5_309	SP0_XS0E_SPARE1
310	5_310	SP0_XS0E_SPARE0
311	5_311	SP0_XS1E_SPARE1
312	5_312	SP0_XS1E_SPARE0
313	5_313	XRE_SP0_SPARE1
314	5_314	XRE_SP0_SPARE0
315	5_315	
316	5_316	
317	5_317	VP0_SP0_PAR<7>
318	5_318	VP0_SP0_DATA<0>
319	5_319	VP0_SP0_DATA<1>
320	5_320	VP0_SP0_PAR<6>
321	5_321	VP0_SP0_DATA<8>
322	5_322	VP0_SP0_DATA<9>
323	5_323	VP0_SP0_PAR<5>
324	5_324	VP0_SP0_DATA<16>
325	5_325	VP0_SP0_DATA<17>
326	5_326	VP0_SP0_PAR<4>
327	5_327	VP0_SP0_DATA<24>
328	5_328	VP0_SP0_DATA<25>
329	5_329	VP0_SP0_PAR<3>
330	5_330	VP0_SP0_DATA<32>
331	5_331	VP0_SP0_DATA<33>
332	5_332	VP0_SP0_PAR<2>
333	5_333	VP0_SP0_DATA<40>
334	5_334	VP0_SP0_DATA<41>
335	5_335	VP0_SP0_PAR<1>
336	5_336	VP0_SP0_DATA<48>
337	5_337	VP0_SP0_DATA<49>
338	5_338	VP0_SP0_PAR<0>
339	5_339	VP0_SP0_DATA<56>
340	5_340	VP0_SP0_DATA<57>

401	5_401	SP0_XC_HARD_ERROR
402	5_402	SP0_VP0_SXV_RDY
403	5_403	SP0_VP0_UX_REQ_NEXT
404	5_404	SP0_VP0_MXV_RDY
405	5_405	SP0_XS00_SPARE1
406	5_406	SP0_XS00_SPARE0
407	5_407	SP0_XS10_SPARE1
408	5_408	SP0_XS10_SPARE0
409	5_409	XRO_SP0_SPARE1
410	5_410	XRO_SP0_SPARE0
411	5_411	
412	5_412	SP0_XC_STOP_CNTR
413	5_413	XC_SP0_SPARE2
414	5_414	XC_SP0_SPARE1
415	5_415	XC_SP0_SPARE0
416	5_416	
417	5_417	SP0_VP0_PAR<7>
418	5_418	SP0_VP0_DATA<0>
419	5_419	SP0_VP0_DATA<1>
420	5_420	SP0_VP0_PAR<6>
421	5_421	SP0_VP0_DATA<8>
422	5_422	SP0_VP0_DATA<9>
423	5_423	SP0_VP0_PAR<5>
424	5_424	SP0_VP0_DATA<16>
425	5_425	SP0_VP0_DATA<17>
426	5_426	SP0_VP0_PAR<4>
427	5_427	SP0_VP0_DATA<24>
428	5_428	SP0_VP0_DATA<25>
429	5_429	SP0_VP0_PAR<3>
430	5_430	SP0_VP0_DATA<32>
431	5_431	SP0_VP0_DATA<33>
432	5_432	SP0_VP0_PAR<2>
433	5_433	SP0_VP0_DATA<40>
434	5_434	SP0_VP0_DATA<41>
435	5_435	SP0_VP0_PAR<1>
436	5_436	SP0_VP0_DATA<48>
437	5_437	SP0_VP0_DATA<49>
438	5_438	SP0_VP0_PAR<0>
439	5_439	SP0_VP0_DATA<56>
440	5_440	SP0_VP0_DATA<57>

501	5_501	
502	5_502	
503	5_503	
504	5_504	
505	5_505	
506	5_506	
507	5_507	
508	5_508	
509	5_509	
510	5_510	
511	5_511	
512	5_512	
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514	5_514	
515	5_515	
516	5_516	
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518	5_518	
519	5_519	
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525	5_525	
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529	5_529	
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531	5_531	
532	5_532	
533	5_533	
534	5_534	
535	5_535	
536	5_536	
537	5_537	
538	5_538	
539	5_539	
540	5_540	GND\G

SECTION 5 (TOP)

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TITLE: CBP
 DRAWING: 411-001286-300A Rev 0.0

ABBR: CBP
 ENGR: GOLENBIESKI

REVISED: Thu Jun 21 09:34:52 1990

PAGE: 11 of 21

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 VP0 1P
 BOARD=NVP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.
 SEC=1

GROUND ALL PINS ON THIS ROW!

101	1_101
102	1_102
103	1_103
104	1_104
105	1_105
106	1_106
107	1_107
108	1_108
109	1_109
110	1_110
111	1_111
112	1_112
113	1_113
114	1_114
115	1_115
116	1_116
117	1_117
118	1_118
119	1_119
120	1_120
121	1_121
122	1_122
123	1_123
124	1_124
125	1_125
126	1_126
127	1_127
128	1_128
129	1_129
130	1_130
131	1_131
132	1_132
133	1_133
134	1_134
135	1_135
136	1_136
137	1_137
138	1_138
139	1_139
140	1_140

BP_VP0.PORTID<3>
 VP0_BP.LBD_INTL_OUT
 EP_VP0.EPTYPE<3>
 EP_VP0.SLOTID<3>
 CU_VP0.CLOCK_3X

201	1_201
202	1_202
203	1_203
204	1_204
205	1_205
206	1_206
207	1_207
208	1_208
209	1_209
210	1_210
211	1_211
212	1_212
213	1_213
214	1_214
215	1_215
216	1_216
217	1_217
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220	1_220
221	1_221
222	1_222
223	1_223
224	1_224
225	1_225
226	1_226
227	1_227
228	1_228
229	1_229
230	1_230
231	1_231
232	1_232
233	1_233
234	1_234
235	1_235
236	1_236
237	1_237
238	1_238
239	1_239
240	1_240

BP_VP0.PORTID<2>
 BP_VP0.LBD_INTL_IN
 EP_VP0.EPTYPE<2>
 EP_VP0.SLOTID<2>
 CU_VP0.CLOCK_3X*

301	1_301
302	1_302
303	1_303
304	1_304
305	1_305
306	1_306
307	1_307
308	1_308
309	1_309
310	1_310
311	1_311
312	1_312
313	1_313
314	1_314
315	1_315
316	1_316
317	1_317
318	1_318
319	1_319
320	1_320
321	1_321
322	1_322
323	1_323
324	1_324
325	1_325
326	1_326
327	1_327
328	1_328
329	1_329
330	1_330
331	1_331
332	1_332
333	1_333
334	1_334
335	1_335
336	1_336
337	1_337
338	1_338
339	1_339
340	1_340

VP0.SP0.IDLE
 BP_VP0.PORTID<1>
 BP_VP0.LBD_INTL_IN
 EP_VP0.EPTYPE<1>
 EP_VP0.SLOTID<1>

401	1_401
402	1_402
403	1_403
404	1_404
405	1_405
406	1_406
407	1_407
408	1_408
409	1_409
410	1_410
411	1_411
412	1_412
413	1_413
414	1_414
415	1_415
416	1_416
417	1_417
418	1_418
419	1_419
420	1_420
421	1_421
422	1_422
423	1_423
424	1_424
425	1_425
426	1_426
427	1_427
428	1_428
429	1_429
430	1_430
431	1_431
432	1_432
433	1_433
434	1_434
435	1_435
436	1_436
437	1_437
438	1_438
439	1_439
440	1_440

SP0_VP0.DISP_EP<10>
 SP0_VP0.DISP_EP<9>
 SP0_VP0.DISP_EP<8>
 SP0_VP0.DISP_EP<7>
 SP0_VP0.DISP_EP<6>
 SP0_VP0.DISP_EP<5>
 SP0_VP0.DISP_EP<4>
 SP0_VP0.DISP_EP<3>
 SP0_VP0.DISP_EP<2>
 SP0_VP0.DISP_EP<1>
 SP0_VP0.DISP_EP<0>
 SP0_VP0.DISP_IREG<2>
 SP0_VP0.DISP_IREG<1>
 SP0_VP0.DISP_IREG<0>
 SP0_VP0.DISP_JREG<2>
 SP0_VP0.DISP_JREG<1>
 SP0_VP0.DISP_JREG<0>
 SP0_VP0.DISP_KREG<2>
 SP0_VP0.DISP_KREG<1>
 SP0_VP0.DISP_KREG<0>
 SP0_VP0.IEEE
 BP_VP0.PORTID<0>
 BP_VP0.EPTYPE<0>
 BP_VP0.SLOTID<0>

501	1_501
502	1_502
503	1_503
504	1_504
505	1_505
506	1_506
507	1_507
508	1_508
509	1_509
510	1_510
511	1_511
512	1_512
513	1_513
514	1_514
515	1_515
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520	1_520
521	1_521
522	1_522
523	1_523
524	1_524
525	1_525
526	1_526
527	1_527
528	1_528
529	1_529
530	1_530
531	1_531
532	1_532
533	1_533
534	1_534
535	1_535
536	1_536
537	1_537
538	1_538
539	1_539
540	1_540

GND\G

CONNECTOR 1 (BOTTOM)

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TITLE: CBP
 DRAWING: 411-001286-300A Rev 0.0
 REVISED: Thu Jun 21 09:35:21 1990

ABBR: CBP
 ENGR: GOLENBIESKI

PAGE: 12 of 21

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 VP0 1P
 BOARD=NVP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.

SEC=2

GROUND ALL PINS ON THIS ROW!

101	2_101
102	2_102
103	2_103
104	2_104
105	2_105
106	2_106
107	2_107
108	2_108
109	2_109
110	2_110
111	2_111
112	2_112
113	2_113
114	2_114
115	2_115
116	2_116
117	2_117
118	2_118
119	2_119
120	2_120
121	2_121
122	2_122
123	2_123
124	2_124
125	2_125
126	2_126
127	2_127
128	2_128
129	2_129
130	2_130
131	2_131
132	2_132
133	2_133
134	2_134
135	2_135
136	2_136
137	2_137 VP0_SP0_SPARE3
138	2_138 VP0_SP0_SPARE4
139	2_139 VP0_SP0_SPARE5
140	2_140 VP0_SP0_SPARE6

201	2_201
202	2_202
203	2_203
204	2_204
205	2_205
206	2_206
207	2_207
208	2_208
209	2_209
210	2_210
211	2_211
212	2_212
213	2_213
214	2_214
215	2_215
216	2_216
217	2_217
218	2_218
219	2_219
220	2_220
221	2_221
222	2_222
223	2_223
224	2_224
225	2_225
226	2_226
227	2_227
228	2_228
229	2_229
230	2_230
231	2_231
232	2_232
233	2_233
234	2_234
235	2_235
236	2_236
237	2_237
238	2_238
239	2_239
240	2_240

301	2_301	VP0_SP0_DATA<5>
302	2_302	VP0_SP0_DATA<6>
303	2_303	VP0_SP0_DATA<7>
304	2_304	VP0_SP0_DATA<13>
305	2_305	VP0_SP0_DATA<14>
306	2_306	VP0_SP0_DATA<15>
307	2_307	VP0_SP0_DATA<21>
308	2_308	VP0_SP0_DATA<22>
309	2_309	VP0_SP0_DATA<23>
310	2_310	VP0_SP0_DATA<29>
311	2_311	VP0_SP0_DATA<30>
312	2_312	VP0_SP0_DATA<31>
313	2_313	VP0_SP0_DATA<37>
314	2_314	VP0_SP0_DATA<38>
315	2_315	VP0_SP0_DATA<39>
316	2_316	VP0_SP0_DATA<45>
317	2_317	VP0_SP0_DATA<46>
318	2_318	VP0_SP0_DATA<47>
319	2_319	VP0_SP0_DATA<53>
320	2_320	VP0_SP0_DATA<54>
321	2_321	VP0_SP0_DATA<55>
322	2_322	VP0_SP0_DATA<61>
323	2_323	VP0_SP0_DATA<62>
324	2_324	VP0_SP0_DATA<63>
325	2_325	
326	2_326	
327	2_327	
328	2_328	
329	2_329	
330	2_330	VP0_SP0_MXV_REQ_NEXT
331	2_331	VP0_SP0_SXV_REQ_NEXT
332	2_332	
333	2_333	VP0_SP0_PSW_HAZ
334	2_334	VP0_SP0_SET_FDZ
335	2_335	VP0_SP0_SET_FSN
336	2_336	VP0_SP0_SET_OV
337	2_337	VP0_SP0_SET_RO
338	2_338	VP0_SP0_SET_SDZ
339	2_339	VP0_SP0_SET_SIV
340	2_340	VP0_SP0_SET_UN

401	2_401	SP0_VP0_DATA<5>
402	2_402	SP0_VP0_DATA<6>
403	2_403	SP0_VP0_DATA<7>
404	2_404	SP0_VP0_DATA<13>
405	2_405	SP0_VP0_DATA<14>
406	2_406	SP0_VP0_DATA<15>
407	2_407	SP0_VP0_DATA<21>
408	2_408	SP0_VP0_DATA<22>
409	2_409	SP0_VP0_DATA<23>
410	2_410	SP0_VP0_DATA<29>
411	2_411	SP0_VP0_DATA<30>
412	2_412	SP0_VP0_DATA<31>
413	2_413	SP0_VP0_DATA<37>
414	2_414	SP0_VP0_DATA<38>
415	2_415	SP0_VP0_DATA<39>
416	2_416	SP0_VP0_DATA<45>
417	2_417	SP0_VP0_DATA<46>
418	2_418	SP0_VP0_DATA<47>
419	2_419	SP0_VP0_DATA<53>
420	2_420	SP0_VP0_DATA<54>
421	2_421	SP0_VP0_DATA<55>
422	2_422	SP0_VP0_DATA<61>
423	2_423	SP0_VP0_DATA<62>
424	2_424	SP0_VP0_DATA<63>
425	2_425	
426	2_426	
427	2_427	
428	2_428	
429	2_429	
430	2_430	
431	2_431	
432	2_432	SP0_VP0_DISP_RDY
433	2_433	SP0_VP0_DISP_PSW_HAZ
434	2_434	
435	2_435	
436	2_436	
437	2_437	
438	2_438	
439	2_439	
440	2_440	

501	2_501
502	2_502
503	2_503
504	2_504
505	2_505
506	2_506
507	2_507
508	2_508
509	2_509
510	2_510
511	2_511
512	2_512
513	2_513
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515	2_515
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526	2_526
527	2_527
528	2_528
529	2_529
530	2_530
531	2_531
532	2_532
533	2_533
534	2_534
535	2_535
536	2_536
537	2_537
538	2_538
539	2_539
540	2_540 GNDNG

CONNECTOR 2

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TITLE: CBP
 DRAWING: 411-001286-300A Rev 0.0
 REVISED: Thu Jun 21 09:35:44 1990

ABBR: CBP
 ENGR: GOLEMBIESKI

PAGE: 13 of 21

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 VP0 1P

BOARD=NVP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.

SEC=3

GROUND ALL PINS ON THIS ROW!

101	3_101	
102	3_102	
103	3_103	
104	3_104	
105	3_105	
106	3_106	
107	3_107	
108	3_108	
109	3_109	
110	3_110	
111	3_111	
112	3_112	
113	3_113	
114	3_114	
115	3_115	
116	3_116	
117	3_117	
118	3_118	
119	3_119	
120	3_120	
121	3_121	
122	3_122	
123	3_123	
124	3_124	
125	3_125	
126	3_126	
127	3_127	
128	3_128	
129	3_129	
130	3_130	
131	3_131	
132	3_132	VP0_SP0_UXA_ADDR_PAR<0>
133	3_133	VP0_SP0_UXA_ADDR<24>
134	3_134	VP0_SP0_UXA_ADDR<25>
135	3_135	VP0_SP0_UXA_ADDR<26>
136	3_136	VP0_SP0_UXA_ADDR<27>
137	3_137	VP0_SP0_UXA_ADDR<28>
138	3_138	VP0_SP0_UXA_ADDR<29>
139	3_139	VP0_SP0_UXA_ADDR<30>
140	3_140	VP0_SP0_UXA_ADDR<31>

201	3_201	
202	3_202	
203	3_203	
204	3_204	
205	3_205	
206	3_206	
207	3_207	
208	3_208	
209	3_209	
210	3_210	
211	3_211	
212	3_212	
213	3_213	
214	3_214	
215	3_215	
216	3_216	
217	3_217	
218	3_218	
219	3_219	
220	3_220	
221	3_221	
222	3_222	
223	3_223	
224	3_224	
225	3_225	
226	3_226	
227	3_227	
228	3_228	
229	3_229	
230	3_230	
231	3_231	
232	3_232	VP0_SP0_UXA_ADDR_PAR<1>
233	3_233	VP0_SP0_UXA_ADDR<16>
234	3_234	VP0_SP0_UXA_ADDR<17>
235	3_235	VP0_SP0_UXA_ADDR<18>
236	3_236	VP0_SP0_UXA_ADDR<19>
237	3_237	VP0_SP0_UXA_ADDR<20>
238	3_238	VP0_SP0_UXA_ADDR<21>
239	3_239	VP0_SP0_UXA_ADDR<22>
240	3_240	VP0_SP0_UXA_ADDR<23>

301	3_301	VP0_SP0_DATA<2>
302	3_302	VP0_SP0_DATA<3>
303	3_303	VP0_SP0_DATA<4>
304	3_304	VP0_SP0_DATA<10>
305	3_305	VP0_SP0_DATA<11>
306	3_306	VP0_SP0_DATA<12>
307	3_307	VP0_SP0_DATA<18>
308	3_308	VP0_SP0_DATA<19>
309	3_309	VP0_SP0_DATA<20>
310	3_310	VP0_SP0_DATA<26>
311	3_311	VP0_SP0_DATA<27>
312	3_312	VP0_SP0_DATA<28>
313	3_313	VP0_SP0_DATA<34>
314	3_314	VP0_SP0_DATA<35>
315	3_315	VP0_SP0_DATA<36>
316	3_316	VP0_SP0_DATA<42>
317	3_317	VP0_SP0_DATA<43>
318	3_318	VP0_SP0_DATA<44>
319	3_319	VP0_SP0_DATA<50>
320	3_320	VP0_SP0_DATA<51>
321	3_321	VP0_SP0_DATA<52>
322	3_322	VP0_SP0_DATA<58>
323	3_323	VP0_SP0_DATA<59>
324	3_324	VP0_SP0_DATA<60>
325	3_325	
326	3_326	
327	3_327	
328	3_328	
329	3_329	
330	3_330	
331	3_331	
332	3_332	
333	3_333	
334	3_334	
335	3_335	
336	3_336	
337	3_337	
338	3_338	
339	3_339	
340	3_340	

401	3_401	SP0_VP0_DATA<2>
402	3_402	SP0_VP0_DATA<3>
403	3_403	SP0_VP0_DATA<4>
404	3_404	SP0_VP0_DATA<10>
405	3_405	SP0_VP0_DATA<11>
406	3_406	SP0_VP0_DATA<12>
407	3_407	SP0_VP0_DATA<18>
408	3_408	SP0_VP0_DATA<19>
409	3_409	SP0_VP0_DATA<20>
410	3_410	SP0_VP0_DATA<26>
411	3_411	SP0_VP0_DATA<27>
412	3_412	SP0_VP0_DATA<28>
413	3_413	SP0_VP0_DATA<34>
414	3_414	SP0_VP0_DATA<35>
415	3_415	SP0_VP0_DATA<36>
416	3_416	SP0_VP0_DATA<42>
417	3_417	SP0_VP0_DATA<43>
418	3_418	SP0_VP0_DATA<44>
419	3_419	SP0_VP0_DATA<50>
420	3_420	SP0_VP0_DATA<51>
421	3_421	SP0_VP0_DATA<52>
422	3_422	SP0_VP0_DATA<58>
423	3_423	SP0_VP0_DATA<59>
424	3_424	SP0_VP0_DATA<60>
425	3_425	
426	3_426	
427	3_427	
428	3_428	
429	3_429	
430	3_430	
431	3_431	
432	3_432	
433	3_433	
434	3_434	
435	3_435	
436	3_436	
437	3_437	
438	3_438	
439	3_439	SP0_VP0_CNTL_CTL<1>
440	3_440	SP0_VP0_CNTL_CTL<0>

501	3_501	
502	3_502	
503	3_503	
504	3_504	
505	3_505	
506	3_506	
507	3_507	
508	3_508	
509	3_509	
510	3_510	
511	3_511	
512	3_512	
513	3_513	
514	3_514	
515	3_515	
516	3_516	
517	3_517	
518	3_518	
519	3_519	
520	3_520	
521	3_521	
522	3_522	
523	3_523	
524	3_524	
525	3_525	
526	3_526	
527	3_527	
528	3_528	
529	3_529	
530	3_530	
531	3_531	
532	3_532	
533	3_533	
534	3_534	
535	3_535	
536	3_536	
537	3_537	
538	3_538	
539	3_539	
540	3_540	GND\G

CONNECTOR 3

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TITLE: CBP
 DRAWING: 411-001285-300A Rev 0.0

ABBR: CBP
 ENGR: GOLENBIESKI

REVISED: Thu Jun 21 09:36:08 1990

PAGE: 14 of 21

AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 VP0 1P
 BOARD=NVP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.

SEC=4

GROUND ALL PINS ON THIS ROW!

101	4_101	
102	4_102	
103	4_103	
104	4_104	
105	4_105	
106	4_106	
107	4_107	
108	4_108	
109	4_109	
110	4_110	
111	4_111	
112	4_112	
113	4_113	
114	4_114	
115	4_115	
116	4_116	
117	4_117	SP0_VP0, SPARE3
118	4_118	SP0_VP0, SPARE2
119	4_119	SP0_VP0, SPARE1
120	4_120	SP0_VP0, SPARE0
121	4_121	
122	4_122	
123	4_123	VP0_SP0, UXA_ADDR<3>
124	4_124	VP0_SP0, UXA_ADDR<0>
125	4_125	VP0_SP0, UXA_ADDR<1>
126	4_126	VP0_SP0, UXA_ADDR<2>
127	4_127	VP0_SP0, UXA_ADDR<3>
128	4_128	VP0_SP0, UXA_ADDR<4>
129	4_129	VP0_SP0, UXA_ADDR<5>
130	4_130	VP0_SP0, UXA_ADDR<6>
131	4_131	VP0_SP0, UXA_ADDR<7>
132	4_132	VP0_SP0, UXA_ADDR<8>
133	4_133	VP0_SP0, UXA_ADDR<9>
134	4_134	VP0_SP0, UXA_ADDR<10>
135	4_135	VP0_SP0, UXA_ADDR<11>
136	4_136	VP0_SP0, UXA_ADDR<12>
137	4_137	VP0_SP0, UXA_ADDR<13>
138	4_138	VP0_SP0, UXA_ADDR<14>
139	4_139	VP0_SP0, UXA_ADDR<15>
140	4_140	VP0_SP0, UXA_ADDR<15>

201	4_201	
202	4_202	
203	4_203	
204	4_204	
205	4_205	
206	4_206	
207	4_207	
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209	4_209	
210	4_210	
211	4_211	
212	4_212	
213	4_213	
214	4_214	
215	4_215	
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217	4_217	
218	4_218	
219	4_219	
220	4_220	
221	4_221	
222	4_222	
223	4_223	
224	4_224	
225	4_225	
226	4_226	
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229	4_229	
230	4_230	
231	4_231	
232	4_232	
233	4_233	
234	4_234	
235	4_235	
236	4_236	
237	4_237	
238	4_238	
239	4_239	
240	4_240	

301	4_301	
302	4_302	
303	4_303	
304	4_304	
305	4_305	
306	4_306	
307	4_307	
308	4_308	
309	4_309	
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311	4_311	
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314	4_314	
315	4_315	
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319	4_319	
320	4_320	
321	4_321	
322	4_322	
323	4_323	
324	4_324	
325	4_325	
326	4_326	
327	4_327	
328	4_328	
329	4_329	
330	4_330	
331	4_331	
332	4_332	
333	4_333	
334	4_334	
335	4_335	
336	4_336	
337	4_337	
338	4_338	
339	4_339	
340	4_340	

401	4_401	
402	4_402	
403	4_403	
404	4_404	
405	4_405	
406	4_406	
407	4_407	
408	4_408	
409	4_409	
410	4_410	
411	4_411	
412	4_412	
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424	4_424	
425	4_425	
426	4_426	
427	4_427	
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429	4_429	
430	4_430	
431	4_431	
432	4_432	
433	4_433	
434	4_434	
435	4_435	
436	4_436	
437	4_437	
438	4_438	
439	4_439	
440	4_440	

501	4_501	
502	4_502	
503	4_503	
504	4_504	
505	4_505	
506	4_506	
507	4_507	
508	4_508	
509	4_509	
510	4_510	
511	4_511	
512	4_512	
513	4_513	
514	4_514	
515	4_515	
516	4_516	
517	4_517	
518	4_518	
519	4_519	
520	4_520	
521	4_521	
522	4_522	
523	4_523	
524	4_524	
525	4_525	
526	4_526	
527	4_527	
528	4_528	
529	4_529	
530	4_530	
531	4_531	
532	4_532	
533	4_533	
534	4_534	
535	4_535	
536	4_536	
537	4_537	
538	4_538	
539	4_539	
540	4_540	

GND\G

CONNECTOR 4

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TITLE: CBP
 DRAWING: 411-001285-300A Rev 0.0

ABBR: CBP
 ENGR: GOLENBIESKI

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AUGAT-NGC-800
 BACKPLANE VERSION
 800 SIGNALS + 200 GROUNDS IN 5 SECTIONS
 VP0 1P
 BOARD=NVP

TOP
 J5
 J4
 J3
 J2
 J1
 BOTTOM

NOTE: CHANGE THE NUMBER BELOW TO CORRESPOND TO DESIRED CONNECTOR SECTION (1=J1, 2=J2, ETC.). THE GED 'SECTION' COMMAND WILL NOT WORK.

SEC=5

GROUND ALL PINS ON THIS ROW!

101	S_101	XC_VP0_SCAN_CTL<2>
102	S_102	XC_VP0_SCAN_IN
103	S_103	
104	S_104	
105	S_105	
106	S_106	
107	S_107	
108	S_108	
109	S_109	
110	S_110	
111	S_111	
112	S_112	
113	S_113	
114	S_114	
115	S_115	
116	S_116	
117	S_117	
118	S_118	
119	S_119	
120	S_120	
121	S_121	
122	S_122	
123	S_123	
124	S_124	
125	S_125	
126	S_126	
127	S_127	
128	S_128	
129	S_129	
130	S_130	
131	S_131	
132	S_132	
133	S_133	
134	S_134	
135	S_135	
136	S_136	
137	S_137	
138	S_138	
139	S_139	
140	S_140	

201	S_201	XC_VP0_SCAN_CTL<1>
202	S_202	VP0_XC_SCAN_OUT
203	S_203	
204	S_204	
205	S_205	
206	S_206	
207	S_207	
208	S_208	
209	S_209	
210	S_210	
211	S_211	
212	S_212	
213	S_213	
214	S_214	
215	S_215	
216	S_216	
217	S_217	
218	S_218	
219	S_219	
220	S_220	
221	S_221	
222	S_222	
223	S_223	
224	S_224	
225	S_225	
226	S_226	
227	S_227	
228	S_228	
229	S_229	
230	S_230	
231	S_231	
232	S_232	
233	S_233	
234	S_234	
235	S_235	
236	S_236	
237	S_237	
238	S_238	
239	S_239	
240	S_240	

301	S_301	XC_VP0_SCAN_CTL<0>
302	S_302	VP0_SP0_DISP_REQ_NEXT
303	S_303	
304	S_304	VP0_SP0_UXM_RDY
305	S_305	VP0_SP0_UXS_RDY
306	S_306	VP0_SP0_UXA_VM<0>
307	S_307	VP0_SP0_UXA_VM<1>
308	S_308	VP0_SP0_UXA_LAST
309	S_309	
310	S_310	
311	S_311	
312	S_312	
313	S_313	
314	S_314	
315	S_315	
316	S_316	
317	S_317	VP0_SP0_PAR<7>
318	S_318	VP0_SP0_DATA<0>
319	S_319	VP0_SP0_DATA<1>
320	S_320	VP0_SP0_PAR<6>
321	S_321	VP0_SP0_DATA<8>
322	S_322	VP0_SP0_DATA<9>
323	S_323	VP0_SP0_PAR<5>
324	S_324	VP0_SP0_DATA<16>
325	S_325	VP0_SP0_DATA<17>
326	S_326	VP0_SP0_PAR<4>
327	S_327	VP0_SP0_DATA<24>
328	S_328	VP0_SP0_DATA<25>
329	S_329	VP0_SP0_PAR<3>
330	S_330	VP0_SP0_DATA<32>
331	S_331	VP0_SP0_DATA<33>
332	S_332	VP0_SP0_PAR<2>
333	S_333	VP0_SP0_DATA<40>
334	S_334	VP0_SP0_DATA<41>
335	S_335	VP0_SP0_PAR<1>
336	S_336	VP0_SP0_DATA<48>
337	S_337	VP0_SP0_DATA<49>
338	S_338	VP0_SP0_PAR<0>
339	S_339	VP0_SP0_DATA<56>
340	S_340	VP0_SP0_DATA<57>

401	S_401	VP0_XC_HARD_ERROR
402	S_402	SP0_VP0_SXV_RDY
403	S_403	SP0_VP0_UX_REQ_NEXT
404	S_404	SP0_VP0_MXV_RDY
405	S_405	
406	S_406	
407	S_407	
408	S_408	
409	S_409	
410	S_410	
411	S_411	
412	S_412	
413	S_413	
414	S_414	
415	S_415	
416	S_416	
417	S_417	SP0_VP0_PAR<7>
418	S_418	SP0_VP0_DATA<0>
419	S_419	SP0_VP0_DATA<1>
420	S_420	SP0_VP0_PAR<6>
421	S_421	SP0_VP0_DATA<8>
422	S_422	SP0_VP0_DATA<9>
423	S_423	SP0_VP0_PAR<5>
424	S_424	SP0_VP0_DATA<16>
425	S_425	SP0_VP0_DATA<17>
426	S_426	SP0_VP0_PAR<4>
427	S_427	SP0_VP0_DATA<24>
428	S_428	SP0_VP0_DATA<25>
429	S_429	SP0_VP0_PAR<3>
430	S_430	SP0_VP0_DATA<32>
431	S_431	SP0_VP0_DATA<33>
432	S_432	SP0_VP0_PAR<2>
433	S_433	SP0_VP0_DATA<40>
434	S_434	SP0_VP0_DATA<41>
435	S_435	SP0_VP0_PAR<1>
436	S_436	SP0_VP0_DATA<48>
437	S_437	SP0_VP0_DATA<49>
438	S_438	SP0_VP0_PAR<0>
439	S_439	SP0_VP0_DATA<56>
440	S_440	SP0_VP0_DATA<57>

501	S_501	
502	S_502	
503	S_503	
504	S_504	
505	S_505	
506	S_506	
507	S_507	
508	S_508	
509	S_509	
510	S_510	
511	S_511	
512	S_512	
513	S_513	
514	S_514	
515	S_515	
516	S_516	
517	S_517	
518	S_518	
519	S_519	
520	S_520	
521	S_521	
522	S_522	
523	S_523	
524	S_524	
525	S_525	
526	S_526	
527	S_527	
528	S_528	
529	S_529	
530	S_530	
531	S_531	
532	S_532	
533	S_533	
534	S_534	
535	S_535	
536	S_536	
537	S_537	
538	S_538	
539	S_539	
540	S_540	GND/G

CONNECTOR 5 (TOP)

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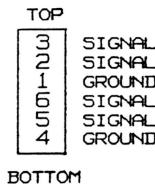


TITLE: CBP
 DRAWING: 411-001286-300A Rev 0.0

ABBR: CBP
 ENGR: GOLEMBIESKI

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DUPONT-204
 CPU OR I/O BAY BACKPLANE TYPE
 J01 1P



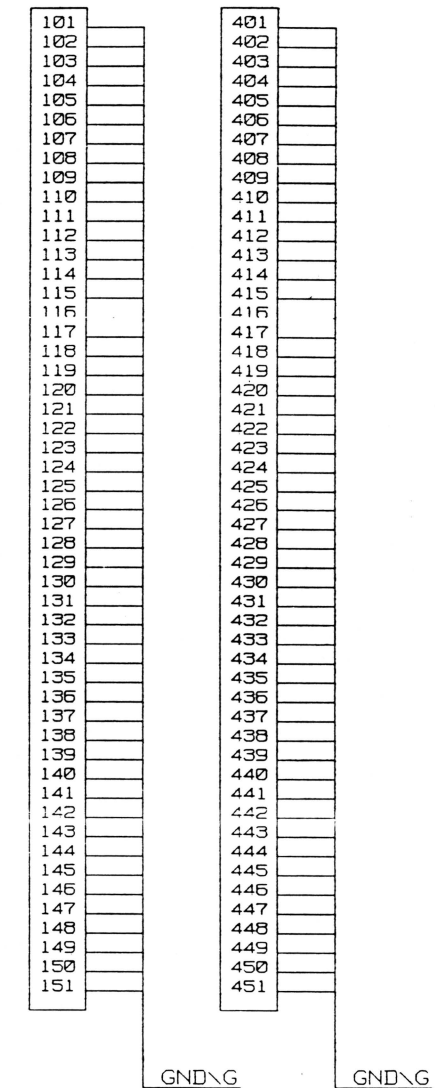
GROUND ALL PINS
 ON THESE TWO ROWS:

201	XRE_SP0.RD_PAR<3>
202	XRE_SP0.RD_PAR<2>
203	XRE_SP0.RD_DATA<25>
204	XRE_SP0.RD_DATA<24>
205	XRE_SP0.RD_DATA<17>
206	XRE_SP0.RD_DATA<16>
207	SP0_XSE.ADDR<28>
208	SP0_XSE.ADDR<27>
209	SP0_XSE.ADDR<26>
210	SP0_XSE.ADDR<25>
211	SP0_XSE.ADDR<24>
212	SP0_XSE.ADDR<23>
213	SP0_XSE.ADDR<22>
214	SP0_XSE.WR_ZONE<3>
215	SP0_XSE.WR_ZONE<2>
216	SP0_XSE.WR_ZONE<1>
217	SP0_XSE.WR_ZONE<0>
218	SP0_XSE.WR_ZONE<0>
219	SP0_XSE.WR_ZONE<0>
220	SP0_XSE.WR_ZONE<0>
221	SP0_XSE.WR_ZONE<0>
222	SP0_XSE.WR_ZONE<0>
223	SP0_XSE.WR_ZONE<0>
224	SP0_XSE.WR_ZONE<0>
225	XC_SP0.SPARE1
226	XC_SP0.SPARE2
227	MB0_XRE.SPARE1
228	MB0_XRE.SPARE0
229	XSOE_MB0.SPARE1
230	XSOE_MB0.SPARE0
231	XSIE_MB0.SPARE1
232	XSIE_MB0.SPARE0
233	MB0_XSIE.SEND_PAR_ERR
234	XSE_MB0.WR_ZONE<3>
235	XSE_MB0.WR_ZONE<2>
236	XSE_MB0.WR_ZONE<1>
237	XSE_MB0.WR_ZONE<0>
238	XSE_MB0.WR_ZONE<0>
239	XSE_MB0.WR_ZONE<0>
240	XSE_MB0.WR_ZONE<0>
241	XSE_MB0.WR_ZONE<0>
242	XSE_MB0.WR_ZONE<0>
243	XSE_MB0.WR_ZONE<0>
244	XSE_MB0.WR_ZONE<0>
245	XSE_MB0.WR_ZONE<0>
246	MB0_XRE.RD_PAR<3>
247	MB0_XRE.RD_PAR<2>
248	MB0_XRE.RD_DATA<25>
249	MB0_XRE.RD_DATA<24>
250	MB0_XRE.RD_DATA<17>
251	MB0_XRE.RD_DATA<16>

301	XRO_SP0.RD_PAR<3>
302	XRO_SP0.RD_PAR<2>
303	XRO_SP0.RD_DATA<25>
304	XRO_SP0.RD_DATA<24>
305	XRO_SP0.RD_DATA<17>
306	XRO_SP0.RD_DATA<16>
307	SP0_XSO.ADDR<28>
308	SP0_XSO.ADDR<27>
309	SP0_XSO.ADDR<26>
310	SP0_XSO.ADDR<25>
311	SP0_XSO.ADDR<24>
312	SP0_XSO.ADDR<23>
313	SP0_XSO.ADDR<22>
314	SP0_XSO.WR_ZONE<3>
315	SP0_XSO.WR_ZONE<2>
316	SP0_XSO.WR_ZONE<1>
317	SP0_XSO.WR_ZONE<0>
318	SP0_XSO.WR_ZONE<0>
319	SP0_XSO.WR_ZONE<0>
320	SP0_XSO.WR_ZONE<0>
321	SP0_XSO.WR_ZONE<0>
322	SP0_XSO.WR_ZONE<0>
323	XRO_SP0.SPARE1
324	XRO_SP0.SPARE0
325	XC_SP0.SPARE1
326	XC_SP0.SPARE0
327	MB0_XRO.SPARE1
328	MB0_XRO.SPARE0
329	XSOO_MB0.SPARE1
330	XSOO_MB0.SPARE0
331	XSIO_MB0.SPARE1
332	XSIO_MB0.SPARE0
333	MB0_XSIO.SEND_PAR_ERR
334	XSO_MB0.WR_ZONE<3>
335	XSO_MB0.WR_ZONE<2>
336	XSO_MB0.WR_ZONE<1>
337	XSO_MB0.WR_ZONE<0>
338	XSO_MB0.WR_ZONE<0>
339	XSO_MB0.WR_ZONE<0>
340	XSO_MB0.WR_ZONE<0>
341	XSO_MB0.WR_ZONE<0>
342	XSO_MB0.WR_ZONE<0>
343	XSO_MB0.WR_ZONE<0>
344	XSO_MB0.WR_ZONE<0>
345	XSO_MB0.WR_ZONE<0>
346	MB0_XRO.RD_PAR<3>
347	MB0_XRO.RD_PAR<2>
348	MB0_XRO.RD_DATA<25>
349	MB0_XRO.RD_DATA<24>
350	MB0_XRO.RD_DATA<17>
351	MB0_XRO.RD_DATA<16>

501	BP_BP.PORTID_0<3>
502	BP_BP.PORTID_0<2>
503	
504	
505	
506	
507	
508	SP0_XRE.RTN_PAR_ERR
509	XRE_SP0.RD_DATA<9>
510	XRE_SP0.RD_DATA<8>
511	XRE_SP0.RD_DATA<1>
512	XRE_SP0.RD_DATA<0>
513	XRE_SP0.RD_PAR<1>
514	XRE_SP0.RD_PAR<0>
515	XRE_SP0.RD_RDY
516	SP0_XSE.WR_ZONE<0>
517	SP0_XSE.WR_ZONE<0>
518	SP0_XSE.WR_ZONE<0>
519	SP0_XSE.WR_ZONE<0>
520	SP0_XSE.WR_ZONE<0>
521	XC_SP0.SCAN_CTL<1>
522	XC_SP0.SCAN_CTL<0>
523	MB0_XRE.RD_DATA<6>
524	MB0_XRE.RD_DATA<5>
525	MB0_XRE.RD_DATA<12>
526	MB0_XRE.RD_DATA<11>
527	MB0_XRE.RD_DATA<10>
528	MB0_XRE.RD_DATA<4>
529	MB0_XRE.RD_DATA<3>
530	MB0_XRE.RD_DATA<2>
531	XC_MB0.SCAN_CTL<1>
532	XC_MB0.SCAN_CTL<0>
533	XSE_MB0.WR_ZONE<10>
534	XSE_MB0.WR_ZONE<4>
535	XSE_MB0.WR_ZONE<3>
536	XSE_MB0.WR_ZONE<2>
537	XSE_MB0.WR_ZONE<9>
538	XSE_MB0.WR_ZONE<8>
539	XSE_MB0.WR_ZONE<1>
540	XSE_MB0.WR_ZONE<0>
541	XSE_MB0.WR_ZONE<0>
542	XSE_MB0.WR_ZONE<0>
543	XSE_MB0.WR_ZONE<0>
544	XSE_MB0.WR_ZONE<0>
545	MB0_XRE.RD_DATA<9>
546	MB0_XRE.RD_DATA<8>
547	MB0_XRE.RD_DATA<1>
548	MB0_XRE.RD_DATA<0>
549	MB0_XRE.RD_PAR<1>
550	MB0_XRE.RD_PAR<0>
551	MB0_XRE.RD_RDY

601	BP_BP.PORTID_0<1>
602	BP_BP.PORTID_0<0>
603	XC_IA.RESET
604	IA_XC.SOFT_ERROR
605	
606	
607	XC_UP0.SCAN_CTL<2>
608	SP0_XRO.RTN_PAR_ERR
609	XRO_SP0.RD_DATA<9>
610	XRO_SP0.RD_DATA<8>
611	XRO_SP0.RD_DATA<1>
612	XRO_SP0.RD_DATA<0>
613	XRO_SP0.RD_PAR<1>
614	XRO_SP0.RD_PAR<0>
615	XRO_SP0.RD_RDY
616	SP0_XSO.WR_ZONE<0>
617	SP0_XSO.WR_ZONE<0>
618	SP0_XSO.WR_ZONE<0>
619	SP0_XSO.WR_ZONE<0>
620	SP0_XSO.WR_ZONE<0>
621	XC_UP0.SCAN_CTL<1>
622	XC_UP0.SCAN_CTL<0>
623	MB0_XRO.RD_DATA<6>
624	MB0_XRO.RD_DATA<5>
625	MB0_XRO.RD_DATA<12>
626	MB0_XRO.RD_DATA<11>
627	MB0_XRO.RD_DATA<10>
628	MB0_XRO.RD_DATA<4>
629	MB0_XRO.RD_DATA<3>
630	MB0_XRO.RD_DATA<2>
631	
632	MB0_XC.HARD_ERROR
633	XSO_MB0.WR_ZONE<10>
634	XSO_MB0.WR_ZONE<4>
635	XSO_MB0.WR_ZONE<3>
636	XSO_MB0.WR_ZONE<2>
637	XSO_MB0.WR_ZONE<9>
638	XSO_MB0.WR_ZONE<8>
639	XSO_MB0.WR_ZONE<1>
640	XSO_MB0.WR_ZONE<0>
641	XSO_MB0.WR_ZONE<0>
642	XSO_MB0.WR_ZONE<0>
643	XSO_MB0.WR_ZONE<0>
644	XSO_MB0.WR_ZONE<0>
645	MB0_XRO.RD_DATA<9>
646	MB0_XRO.RD_DATA<8>
647	MB0_XRO.RD_DATA<1>
648	MB0_XRO.RD_DATA<0>
649	MB0_XRO.RD_PAR<1>
650	MB0_XRO.RD_PAR<0>
651	MB0_XRO.RD_RDY



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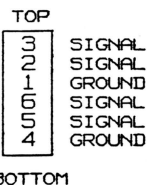
TITLE: CBP
 DRAWING: 411-001286-300A Rev 0.0

ABBR: CBP
 ENGR: GOLENBIESKI

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DUPONT-204
 CPU OR I/O BAY BACKPLANE TYPE
 J02 1P



SIGNAL
 SIGNAL
 GROUND
 SIGNAL
 SIGNAL
 GROUND

GROUND ALL PINS
 ON THESE TWO ROWS!

201	XRE_SP0.RD_DATA<28>
202	XRE_SP0.RD_DATA<27>
203	XRE_SP0.RD_DATA<26>
204	XRE_SP0.RD_DATA<20>
205	XRE_SP0.RD_DATA<19>
206	XRE_SP0.RD_DATA<18>
207	XRE_SP0.RD_DATA<31>
208	XRE_SP0.RD_DATA<30>
209	SP0_XSE.ADDR<21>
210	SP0_XSE.ADDR<20>
211	SP0_XSE.ADDR<19>
212	SP0_XSE.ADDR<18>
213	SP0_XSE.ADDR<17>
214	SP0_XSE.ADDR<16>
215	SP0_XSE.ADDR<15>
216	SP0_XSE.WR_DATA<25>
217	SP0_XSE.WR_DATA<24>
218	SP0_XSE.WR_DATA<17>
219	SP0_XSE.WR_DATA<16>
220	SP0_XSE.WR_DATA<28>
221	SP0_XSE.WR_DATA<27>
222	SP0_XSE.WR_DATA<26>
223	NC
224	NC
225	XC_IA.CCU_RBE<3>
226	XC_IA.CCU_RBE<2>
227	XC_IA.SLOG_ENA
228	XC_IA.CCU_CNTRL_ENA
229	
230	XSE_MB0.WR_DATA<25>
231	XSE_MB0.WR_DATA<24>
232	XSE_MB0.WR_DATA<17>
233	XSE_MB0.WR_DATA<16>
234	XSE_MB0.WR_DATA<28>
235	XSE_MB0.WR_DATA<27>
236	XSE_MB0.WR_DATA<26>
237	XSE_MB0.ADDR<21>
238	XSE_MB0.ADDR<20>
239	XSE_MB0.ADDR<19>
240	XSE_MB0.ADDR<18>
241	XSE_MB0.ADDR<17>
242	XSE_MB0.ADDR<16>
243	XSE_MB0.ADDR<15>
244	MB0_XRE.RD_DATA<28>
245	MB0_XRE.RD_DATA<27>
246	MB0_XRE.RD_DATA<26>
247	MB0_XRE.RD_DATA<20>
248	MB0_XRE.RD_DATA<19>
249	MB0_XRE.RD_DATA<18>
250	MB0_XRE.RD_DATA<31>
251	MB0_XRE.RD_DATA<30>

301	XRO_SP0.RD_DATA<28>
302	XRO_SP0.RD_DATA<27>
303	XRO_SP0.RD_DATA<26>
304	XRO_SP0.RD_DATA<20>
305	XRO_SP0.RD_DATA<19>
306	XRO_SP0.RD_DATA<18>
307	XRO_SP0.RD_DATA<31>
308	XRO_SP0.RD_DATA<30>
309	SP0_XSO.ADDR<21>
310	SP0_XSO.ADDR<20>
311	SP0_XSO.ADDR<19>
312	SP0_XSO.ADDR<18>
313	SP0_XSO.ADDR<17>
314	SP0_XSO.ADDR<16>
315	SP0_XSO.ADDR<15>
316	SP0_XSO.WR_DATA<25>
317	SP0_XSO.WR_DATA<24>
318	SP0_XSO.WR_DATA<17>
319	SP0_XSO.WR_DATA<16>
320	SP0_XSO.WR_DATA<28>
321	SP0_XSO.WR_DATA<27>
322	SP0_XSO.WR_DATA<26>
323	NC
324	NC
325	XC_IA.CCU_RBE<1>
326	XC_IA.CCU_RBE<0>
327	XC_IA.CCU_CLEAR
328	XC_IA.CLOCK_SYNC
329	
330	XSO_MB0.WR_DATA<25>
331	XSO_MB0.WR_DATA<24>
332	XSO_MB0.WR_DATA<17>
333	XSO_MB0.WR_DATA<16>
334	XSO_MB0.WR_DATA<28>
335	XSO_MB0.WR_DATA<27>
336	XSO_MB0.WR_DATA<26>
337	XSO_MB0.ADDR<21>
338	XSO_MB0.ADDR<20>
339	XSO_MB0.ADDR<19>
340	XSO_MB0.ADDR<18>
341	XSO_MB0.ADDR<17>
342	XSO_MB0.ADDR<16>
343	XSO_MB0.ADDR<15>
344	MB0_XRO.RD_DATA<28>
345	MB0_XRO.RD_DATA<27>
346	MB0_XRO.RD_DATA<26>
347	MB0_XRO.RD_DATA<20>
348	MB0_XRO.RD_DATA<19>
349	MB0_XRO.RD_DATA<18>
350	MB0_XRO.RD_DATA<31>
351	MB0_XRO.RD_DATA<30>

501	XRE_SP0.RD_DATA<6>
502	XRE_SP0.RD_DATA<5>
503	XRE_SP0.RD_DATA<12>
504	XRE_SP0.RD_DATA<11>
505	XRE_SP0.RD_DATA<10>
506	XRE_SP0.RD_DATA<4>
507	XRE_SP0.RD_DATA<3>
508	XRE_SP0.RD_DATA<2>
509	XSE_SP0.B_REQ_NEXT
510	XSE_SP0.A_REQ_PEND
511	XSE_SP0.A_ST_PEND
512	SP0_XSE.WR_DATA<10>
513	SP0_XSE.WR_DATA<4>
514	SP0_XSE.WR_DATA<3>
515	SP0_XSE.WR_DATA<2>
516	SP0_XSE.WR_DATA<9>
517	SP0_XSE.WR_DATA<8>
518	SP0_XSE.WR_DATA<1>
519	XC_SP0.USE_CEN
520	XC_SP0.TRAP_VECT<11>
521	XC_SP0.TRAP_VECT<10>
522	XC_SP0.TRAP_VECT<9>
523	XC_SP0.TRAP_VECT<8>
524	XC_SP0.TRAP_VECT<7>
525	XC_SP0.TRAP_VECT<6>
526	XC_SP0.TRAP_TYPE<3>
527	XC_SP0.TRAP_TYPE<2>
528	SP0_XC.TRAP_COMP
529	SP0_XC.DEADLOCK
530	XC_SP0.CU_STATUS
531	XC_MB0.SCAN_CTL<2>
532	XSE_MB0.RDY
533	XSE_MB0.REF_REQ
534	
535	MB0_XSE.BANK_DONE<15>
536	MB0_XSE.BANK_DONE<14>
537	MB0_XSE.BANK_DONE<13>
538	MB0_XSE.BANK_DONE<12>
539	MB0_XSE.BANK_DONE<11>
540	MB0_XSE.BANK_DONE<10>
541	MB0_XSE.BANK_DONE<9>
542	MB0_XSE.BANK_DONE<8>
543	MB0_XSE.BANK_DONE<7>
544	MB0_XSE.BANK_DONE<6>
545	MB0_XSE.BANK_DONE<5>
546	MB0_XSE.BANK_DONE<4>
547	MB0_XSE.BANK_DONE<3>
548	MB0_XSE.BANK_DONE<2>
549	MB0_XSE.BANK_DONE<1>
550	MB0_XSE.BANK_DONE<0>
551	MB0_XSOE.SEND_PAR_ERR

601	XRO_SP0.RD_DATA<6>
602	XRO_SP0.RD_DATA<5>
603	XRO_SP0.RD_DATA<12>
604	XRO_SP0.RD_DATA<11>
605	XRO_SP0.RD_DATA<10>
606	XRO_SP0.RD_DATA<4>
607	XRO_SP0.RD_DATA<3>
608	XRO_SP0.RD_DATA<2>
609	XSO_SP0.B_REQ_NEXT
610	XSO_SP0.A_REQ_PEND
611	XSO_SP0.A_ST_PEND
612	SP0_XSO.WR_DATA<10>
613	SP0_XSO.WR_DATA<4>
614	SP0_XSO.WR_DATA<3>
615	SP0_XSO.WR_DATA<2>
616	SP0_XSO.WR_DATA<9>
617	SP0_XSO.WR_DATA<8>
618	SP0_XSO.WR_DATA<1>
619	XC_SP0.TRAP_VECT<5>
620	XC_SP0.TRAP_VECT<4>
621	XC_SP0.TRAP_VECT<3>
622	XC_SP0.TRAP_VECT<2>
623	XC_SP0.TRAP_VECT<1>
624	XC_SP0.TRAP_VECT<0>
625	UP0_XC.HARD_ERROR
626	XC_SP0.TRAP_TYPE<1>
627	XC_SP0.TRAP_TYPE<0>
628	XC_SP0.TRAP_RDY
629	XC_SP0.MT_COMP
630	XC_SP0.CU_STATUS_EN
631	SP0_XC.HARD_ERROR
632	XC_SP0.SCAN_CTL<2>
633	XSO_MB0.RDY
634	XSO_MB0.REF_REQ
635	MB0_XSO.BANK_DONE<15>
636	MB0_XSO.BANK_DONE<14>
637	MB0_XSO.BANK_DONE<13>
638	MB0_XSO.BANK_DONE<12>
639	MB0_XSO.BANK_DONE<11>
640	MB0_XSO.BANK_DONE<10>
641	MB0_XSO.BANK_DONE<9>
642	MB0_XSO.BANK_DONE<8>
643	MB0_XSO.BANK_DONE<7>
644	MB0_XSO.BANK_DONE<6>
645	MB0_XSO.BANK_DONE<5>
646	MB0_XSO.BANK_DONE<4>
647	MB0_XSO.BANK_DONE<3>
648	MB0_XSO.BANK_DONE<2>
649	MB0_XSO.BANK_DONE<1>
650	MB0_XSO.BANK_DONE<0>
651	MB0_XSOE.SEND_PAR_ERR

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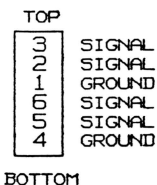
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 ENGR: GOLENBIESKI

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DUPONT-204
CPU OR I/O BAY BACKPLANE TYPE
J03 1P



GROUND ALL PINS
ON THESE TWO ROWS!

201	SP0_XSE.ADDR<14>
202	SP0_XSE.ADDR<13>
203	SP0_XSE.ADDR<12>
204	SP0_XSE.ADDR<11>
205	SP0_XSE.ADDR<10>
206	SP0_XSE.ADDR<9>
207	SP0_XSE.ADDR<8>
208	SP0_XSE.CYCLE<1>
209	SP0_XSE.ADDR<6>
210	SP0_XSE.ADDR<5>
211	SP0_XSE.ADDR<4>
212	SP0_XSE.ADDR<3>
213	SP0_XSE.WR_DATA<20>
214	SP0_XSE.WR_DATA<19>
215	SP0_XSE.WR_DATA<18>
216	SP0_XSE.CTL_PAR<3>
217	SP0_XSE.CTL_PAR<2>
218	SP0_XSE.WR_DATA<31>
219	SP0_XSE.WR_DATA<30>
220	SP0_XSE.WR_DATA<29>
221	SP0_XSE.WR_DATA<23>
222	SP0_XSE.WR_DATA<22>
223	SP0_XSE.WR_DATA<21>
224	SP0_XSE.WR_DATA<15>
225	
226	
227	XSE_MB0.WR_DATA<20>
228	XSE_MB0.WR_DATA<19>
229	XSE_MB0.WR_DATA<18>
230	XSE_MB0.CTL_PAR<3>
231	XSE_MB0.CTL_PAR<2>
232	XSE_MB0.WR_DATA<31>
233	XSE_MB0.WR_DATA<30>
234	XSE_MB0.WR_DATA<29>
235	XSE_MB0.WR_DATA<23>
236	XSE_MB0.WR_DATA<22>
237	XSE_MB0.WR_DATA<21>
238	XSE_MB0.WR_DATA<15>
239	XSE_MB0.WR_DATA<14>
240	XSE_MB0.ADDR<14>
241	XSE_MB0.ADDR<13>
242	XSE_MB0.ADDR<12>
243	XSE_MB0.ADDR<11>
244	XSE_MB0.ADDR<10>
245	XSE_MB0.ADDR<9>
246	XSE_MB0.ADDR<8>
247	XSE_MB0.ADDR<4>
248	XSE_MB0.ADDR<3>
249	XSE_MB0.CYCLE<1>
250	XSE_MB0.ADDR<6>
251	XSE_MB0.ADDR<5>

301	SP0_XSO.ADDR<14>
302	SP0_XSO.ADDR<13>
303	SP0_XSO.ADDR<12>
304	SP0_XSO.ADDR<11>
305	SP0_XSO.ADDR<10>
306	SP0_XSO.ADDR<9>
307	SP0_XSO.ADDR<8>
308	SP0_XSO.CYCLE<1>
309	SP0_XSO.ADDR<6>
310	SP0_XSO.ADDR<5>
311	SP0_XSO.ADDR<4>
312	SP0_XSO.ADDR<3>
313	SP0_XSO.WR_DATA<20>
314	SP0_XSO.WR_DATA<19>
315	SP0_XSO.WR_DATA<18>
316	SP0_XSO.CTL_PAR<3>
317	SP0_XSO.CTL_PAR<2>
318	SP0_XSO.WR_DATA<31>
319	SP0_XSO.WR_DATA<30>
320	SP0_XSO.WR_DATA<29>
321	SP0_XSO.WR_DATA<23>
322	SP0_XSO.WR_DATA<22>
323	SP0_XSO.WR_DATA<21>
324	SP0_XSO.WR_DATA<15>
325	
326	
327	XSO_MB0.WR_DATA<20>
328	XSO_MB0.WR_DATA<19>
329	XSO_MB0.WR_DATA<18>
330	XSO_MB0.CTL_PAR<3>
331	XSO_MB0.CTL_PAR<2>
332	XSO_MB0.WR_DATA<31>
333	XSO_MB0.WR_DATA<30>
334	XSO_MB0.WR_DATA<29>
335	XSO_MB0.WR_DATA<23>
336	XSO_MB0.WR_DATA<22>
337	XSO_MB0.WR_DATA<21>
338	XSO_MB0.WR_DATA<15>
339	XSO_MB0.WR_DATA<14>
340	XSO_MB0.ADDR<14>
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344	XSO_MB0.ADDR<10>
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346	XSO_MB0.ADDR<8>
347	XSO_MB0.ADDR<4>
348	XSO_MB0.ADDR<3>
349	XSO_MB0.CYCLE<1>
350	XSO_MB0.ADDR<6>
351	XSO_MB0.ADDR<5>

501	SP0_XC.STOP_CNTR
502	SP0_XC.SCAN_OUT
503	XC_SP0.SCAN_IN
504	XRE_SP0.RD_DATA<29>
505	XRE_SP0.RD_DATA<23>
506	XRE_SP0.RD_DATA<22>
507	XRE_SP0.RD_DATA<21>
508	XRE_SP0.RD_DATA<15>
509	XRE_SP0.RD_DATA<14>
510	XRE_SP0.RD_DATA<13>
511	XRE_SP0.RD_DATA<7>
512	SP0_XSE.ADDR<7>
513	SP0_XSE.CYCLE<0>
514	XSE_SP0.A_REQ_NEXT
515	XSE_SP0.B_REQ_PEND
516	XSE_SP0.B_ST_PEND
517	SP0_XSE.RDY
518	SP0_XSE.BD_SEL<3>
519	SP0_XSE.BD_SEL<2>
520	SP0_XSE.BD_SEL<1>
521	SP0_XSE.BD_SEL<0>
522	SP0_XSE.WR_DATA<14>
523	SP0_XSE.WR_DATA<13>
524	SP0_XSE.WR_DATA<7>
525	SP0_XSE.WR_DATA<6>
526	SP0_XSE.WR_DATA<5>
527	SP0_XSE.CTL_PAR<1>
528	SP0_XSE.CTL_PAR<0>
529	SP0_XSE.WR_DATA<12>
530	SP0_XSE.WR_DATA<11>
531	-XC_MB0.SYS_RUN
532	MB0_XC.SOFT_ERROR
533	XC_MB0.SCAN_IN
534	XSE_MB0.WR_DATA<13>
535	XSE_MB0.WR_DATA<7>
536	XSE_MB0.WR_DATA<6>
537	XSE_MB0.WR_DATA<5>
538	XSE_MB0.CTL_PAR<1>
539	XSE_MB0.CTL_PAR<0>
540	XSE_MB0.WR_DATA<12>
541	XSE_MB0.WR_DATA<11>
542	XSE_MB0.ADDR<7>
543	XSE_MB0.CYCLE<0>
544	MB0_XRE.RD_DATA<29>
545	MB0_XRE.RD_DATA<23>
546	MB0_XRE.RD_DATA<22>
547	MB0_XRE.RD_DATA<21>
548	MB0_XRE.RD_DATA<15>
549	MB0_XRE.RD_DATA<14>
550	MB0_XRE.RD_DATA<13>
551	MB0_XRE.RD_DATA<7>

601	UP0_XC.SCAN_OUT
602	XC_UP0.SCAN_IN
603	XRO_SP0.RD_DATA<29>
604	XRO_SP0.RD_DATA<23>
605	XRO_SP0.RD_DATA<22>
606	XRO_SP0.RD_DATA<21>
607	XRO_SP0.RD_DATA<15>
608	XRO_SP0.RD_DATA<14>
609	XRO_SP0.RD_DATA<13>
610	XRO_SP0.RD_DATA<7>
611	SP0_XSO.ADDR<7>
612	SP0_XSO.CYCLE<0>
613	XSO_SP0.A_REQ_NEXT
614	XSO_SP0.B_REQ_PEND
615	XSO_SP0.B_ST_PEND
616	SP0_XSO.RDY
617	SP0_XSO.BD_SEL<3>
618	SP0_XSO.BD_SEL<2>
619	SP0_XSO.BD_SEL<1>
620	SP0_XSO.BD_SEL<0>
621	SP0_XSO.WR_DATA<14>
622	SP0_XSO.WR_DATA<13>
623	SP0_XSO.WR_DATA<7>
624	SP0_XSO.WR_DATA<6>
625	SP0_XSO.WR_DATA<5>
626	SP0_XSO.CTL_PAR<1>
627	SP0_XSO.CTL_PAR<0>
628	SP0_XSO.WR_DATA<12>
629	SP0_XSO.WR_DATA<11>
630	-XC_MB0.LOG_RUN
631	XC_MB0.RAM_RFSH
632	MB0_XC.SCAN_OUT
633	XSO_MB0.WR_DATA<13>
634	XSO_MB0.WR_DATA<7>
635	XSO_MB0.WR_DATA<6>
636	XSO_MB0.WR_DATA<5>
637	XSO_MB0.CTL_PAR<1>
638	XSO_MB0.CTL_PAR<0>
639	XSO_MB0.WR_DATA<12>
640	XSO_MB0.WR_DATA<11>
641	XSO_MB0.ADDR<7>
642	XSO_MB0.CYCLE<0>
643	MB0_XRO.RD_DATA<29>
644	MB0_XRO.RD_DATA<23>
645	MB0_XRO.RD_DATA<22>
646	MB0_XRO.RD_DATA<21>
647	MB0_XRO.RD_DATA<15>
648	MB0_XRO.RD_DATA<14>
649	MB0_XRO.RD_DATA<13>
650	MB0_XRO.RD_DATA<7>
651	

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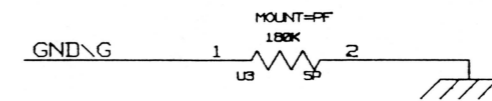
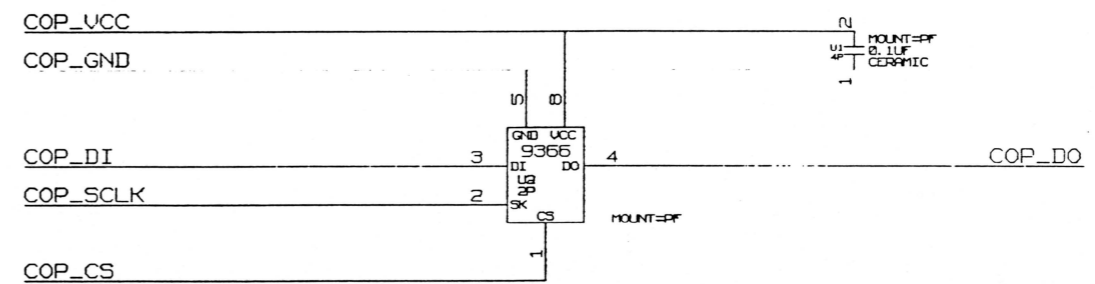
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C3 CLOCK CONNECTOR
 12 PIN STRAIGHT, 3X4 ROW
 (LSR VIEWED FROM INSIDE CABINAGE)

J4	
1P	
LEFT	
1	1 CU_MB0.CLOCK_2X
2	2 CU_MB0.CLOCK_2X*
4	4 CU_SP0.CLOCK_2X
5	5 CU_SP0.CLOCK_2X*
7	7 CU_UP0.CLOCK_3X
8	8 CU_UP0.CLOCK_3X*
10	10 NC
11	11 NC
RIGHT	

HDR10
 301-000035-004
 MALE-PRESSFIT-STRAIGHT-4 WALL-LONG EJECTOR
 J6 3P

1	1 COP_UCC	2	2 COP_CS
3	3 BPTYPE<3>	4	4 COP_SCLK
5	5 BPTYPE<2>	6	6 COP_DI
7	7 BPTYPE<1>	8	8 COP_DO
9	9 BPTYPE<0>	10	10 COP_GND



RESISTOR CONNECTS CHASSIS GND TO SIGNAL GND

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SYNONYMS

12P
 BP_BP.PORTID_0<3> — BP_MB0.PORTID<3>

11P
 BP_BP.PORTID_0<2> — BP_MB0.PORTID<2>

10P
 BP_BP.PORTID_0<1> — BP_MB0.PORTID<1>

9P
 BP_BP.PORTID_0<0> — BP_MB0.PORTID<0>

8P
 BP_BP.PORTID_0<3> — BP_SP0.PORTID<3>

7P
 BP_BP.PORTID_0<2> — BP_SP0.PORTID<2>

6P
 BP_BP.PORTID_0<1> — BP_SP0.PORTID<1>

5P
 BP_BP.PORTID_0<0> — BP_SP0.PORTID<0>

4P
 BP_BP.PORTID_0<3> — BP_UP0.PORTID<3>

3P
 BP_BP.PORTID_0<2> — BP_UP0.PORTID<2>

2P
 BP_BP.PORTID_0<1> — BP_UP0.PORTID<1>

1P
 BP_BP.PORTID_0<0> — BP_UP0.PORTID<0>

29P
 MB0_BP.LBD_INTL_OUT — BP_MB0.LBD_INTL_IN

30P
 SP0_BP.LBD_INTL_OUT — BP_SP0.LBD_INTL_IN

31P
 VP0_BP.LBD_INTL_OUT — BP_UP0.LBD_INTL_IN

21P
 BPTYPE<3> — COP_GND

22P
 BPTYPE<2> — COP_GND

23P
 BPTYPE<1> — NC

24P
 BPTYPE<0> — COP_GND

CPU LEFT BPTYPE = 0X2

25P
 BP_MB0.SLOTID<3> — GND\G

26P
 BP_MB0.SLOTID<2> —

27P
 BP_MB0.SLOTID<1> —

28P
 BP_MB0.SLOTID<0> — GND\G

MB0 SLOTID = 0X6

17P
 BP_SP0.SLOTID<3> — GND\G

18P
 BP_SP0.SLOTID<2> —

19P
 BP_SP0.SLOTID<1> —

20P
 BP_SP0.SLOTID<0> —

SP0 SLOTID = 0X7

13P
 BP_UP0.SLOTID<3> —

14P
 BP_UP0.SLOTID<2> — GND\G

15P
 BP_UP0.SLOTID<1> — GND\G

16P
 BP_UP0.SLOTID<0> — GND\G

VP0 SLOTID = 0X8

C

B

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D

C

B

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